

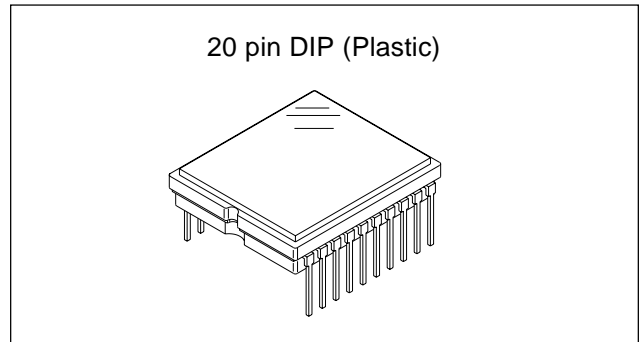
**Diagonal 9.04mm (Type 1/1.8) Frame Readout CCD Image Sensor with a Square Pixel for Color Cameras**

**Description**

The ICX452AQ is a diagonal 9.04mm (Type 1/1.8) interline CCD solid-state image sensor with a square pixel array and 5.13M effective pixels. Adoption of a 3-field readout system ensures small size and high performance. This chip features an electronic shutter with variable charge-storage time.

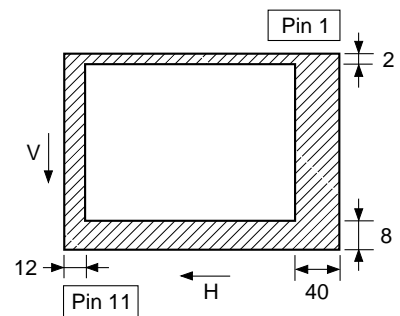
R, G, B primary color mosaic filters are used as the color filters, and at the same time high sensitivity and low dark current are achieved through the adoption of Super HAD CCD technology.

This chip is suitable for applications such as image input of high resolution digital still camera and multimedia system, etc.



**Features**

- Supports frame readout system
- High horizontal and vertical resolution
- Supports high frame rate readout mode: 30 frames/s, AF mode: 60 frames/s, 50 frames/s
- Square pixel
- Horizontal drive frequency: 24.3MHz
- No voltage adjustments (reset gate and substrate bias are not adjusted.)
- R, G, B primary color mosaic filters on chip
- High sensitivity, low dark current
- High resolution, high color reproductivity
- Continuous variable-speed shutter
- Excellent anti-blooming characteristics
- 20-pin high-precision plastic package



**Optical black position (Top View)**

**Device Structure**

- Interline CCD image sensor
- Image size diagonal: 9.04mm (Type 1/1.8)
- Total number of pixels: 2668 (H) × 1970 (V) approx. 5.25M pixels
- Number of effective pixels: 2616 (H) × 1960 (V) approx. 5.13M pixels
- Number of active pixels: 2608 (H) × 1952 (V) approx. 5.09M pixels diagonal 9.040mm
- Number of recommended recording pixels: 2592 (H) × 1944 (V) approx. 5.04M pixels diagonal 8.991mm aspect ratio 4:3
- Chip size: 8.23mm (H) × 6.68mm (V)
- Unit cell size: 2.775µm (H) × 2.775µm (V)
- Optical black: Horizontal (H) direction: Front 12 pixels, rear 40 pixels  
Vertical (V) direction: Front 8 pixels, rear 2 pixels
- Number of dummy bits: Horizontal 28  
Vertical 1 (3rd field only)
- Substrate material: Silicon

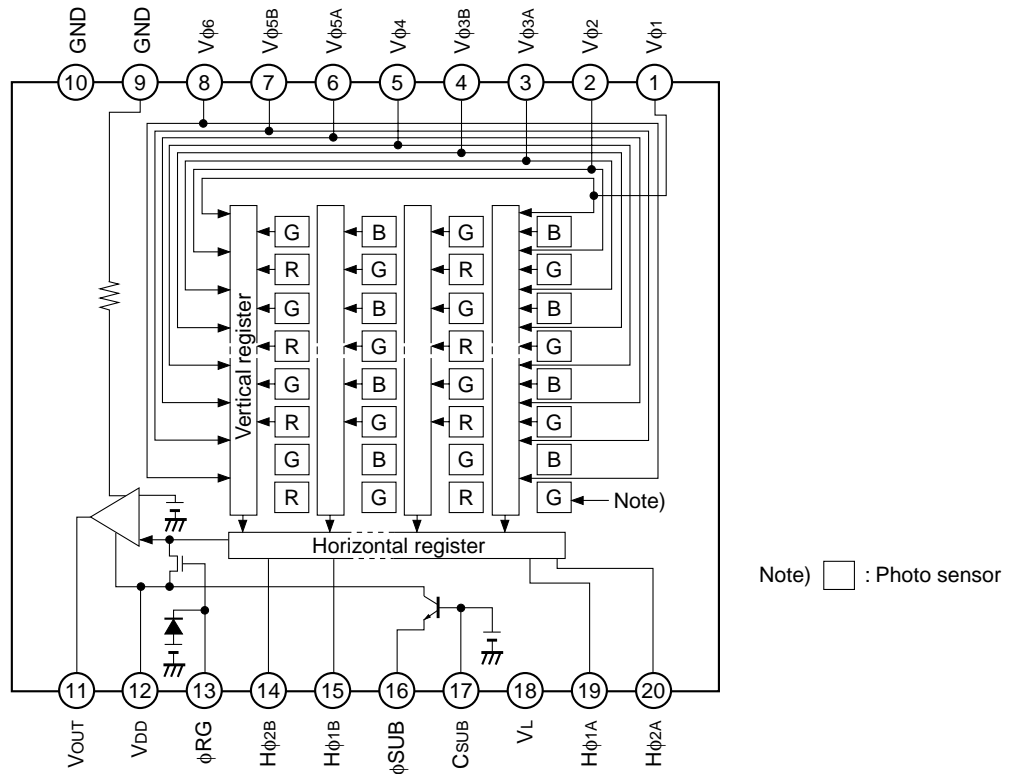
**Super HAD CCD™**

\* Super HAD CCD is a trademark of Sony Corporation. The Super HAD CCD is a version of Sony's high performance CCD HAD (Hole-Accumulation Diode) sensor with sharply improved sensitivity by the incorporation of a new semiconductor technology developed by Sony Corporation.

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**Block Diagram and Pin Configuration**

(Top View)



**Pin Description**

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	Vφ1	Vertical register transfer clock	11	VOUT	Signal output
2	Vφ2	Vertical register transfer clock	12	VDD	Supply voltage
3	Vφ3A	Vertical register transfer clock	13	φRG	Reset gate clock
4	Vφ3B	Vertical register transfer clock	14	Hφ2B	Horizontal register transfer clock
5	Vφ4	Vertical register transfer clock	15	Hφ1B	Horizontal register transfer clock
6	Vφ5A	Vertical register transfer clock	16	φSUB	Substrate clock
7	Vφ5B	Vertical register transfer clock	17	CSUB	Substrate bias*1
8	Vφ6	Vertical register transfer clock	18	VL	Protective transistor bias
9	GND	GND	19	Hφ1A	Horizontal register transfer clock
10	GND	GND	20	Hφ2A	Horizontal register transfer clock

\*1 DC bias is generated within the CCD, so that this pin should be grounded externally through a capacitance of 0.1μF.

## Absolute Maximum Ratings

Item		Ratings	Unit	Remarks
Against $\phi$ SUB	$V_{DD}$ , $V_{OUT}$ , $\phi$ RG – $\phi$ SUB	–40 to +12	V	
	$V\phi_1$ , $V\phi_{3A}$ , $V\phi_{3B}$ , $V\phi_{5A}$ , $V\phi_{5B}$ – $\phi$ SUB	–50 to +15	V	
	$V\phi_2$ , $V\phi_4$ , $V\phi_6$ , $V_L$ – $\phi$ SUB	–50 to +0.3	V	
	$H\phi_{1A}$ , $H\phi_{1B}$ , $H\phi_{2A}$ , $H\phi_{2B}$ , GND – $\phi$ SUB	–40 to +0.3	V	
	$C_{SUB}$ – $\phi$ SUB	–25 to	V	
Against GND	$V_{DD}$ , $V_{OUT}$ , $\phi$ RG, $C_{SUB}$ – GND	–0.3 to +22	V	
	$V\phi_1$ , $V\phi_2$ , $V\phi_{3A}$ , $V\phi_{3B}$ , $V\phi_4$ , $V\phi_{5A}$ , $V\phi_{5B}$ , $V\phi_6$ – GND	–10 to +18	V	
	$H\phi_{1A}$ , $H\phi_{1B}$ , $H\phi_{2A}$ , $H\phi_{2B}$ – GND	–10 to +6.5	V	
Against $V_L$	$V\phi_1$ , $V\phi_{3A}$ , $V\phi_{3B}$ , $V\phi_{5A}$ , $V\phi_{5B}$ – $V_L$	–0.3 to +28	V	
	$V\phi_2$ , $V\phi_4$ , $V\phi_6$ , $H\phi_{1A}$ , $H\phi_{1B}$ , $H\phi_{2A}$ , $H\phi_{2B}$ , GND – $V_L$	–0.3 to +15	V	
Between input clock pins	Voltage difference between vertical clock input pins	to +15	V	*1
	$H\phi_{1A}$ , $H\phi_{1B}$ – $H\phi_{2A}$ , $H\phi_{2B}$	–6.5 to +6.5	V	
	$H\phi_{1A}$ , $H\phi_{1B}$ , $H\phi_{2A}$ , $H\phi_{2B}$ – $V\phi_6$	–10 to +16	V	
Storage temperature		–30 to +80	°C	
Guaranteed temperature of performance		–10 to +60	°C	
Operating temperature		–10 to +75	°C	

\*1 +24V (Max.) when clock width < 10 $\mu$ s, clock duty factor < 0.1%.

+16V (Max.) is guaranteed for turning on or off power supply.

## Bias Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage	V <sub>DD</sub>	14.55	15.0	15.45	V	
Protective transistor bias	V <sub>L</sub>	*1				
Substrate clock	φ <sub>SUB</sub>	*2				
Reset gate clock	φ <sub>RG</sub>	*2				

\*1 V<sub>L</sub> setting is the V<sub>VL</sub> voltage of the vertical clock waveform, or the same voltage as the V<sub>L</sub> power supply for the V driver should be used.

\*2 Do not apply a DC bias to the substrate clock and reset gate clock pins, because a DC bias is generated within the CCD.

## DC Characteristics

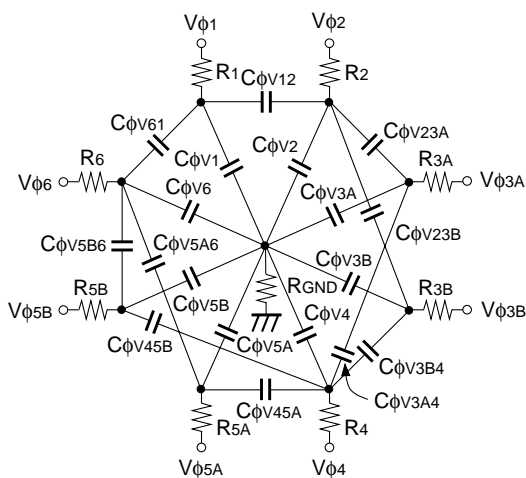
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply current	I <sub>DD</sub>	4	7	10	mA	

## Clock Voltage Conditions

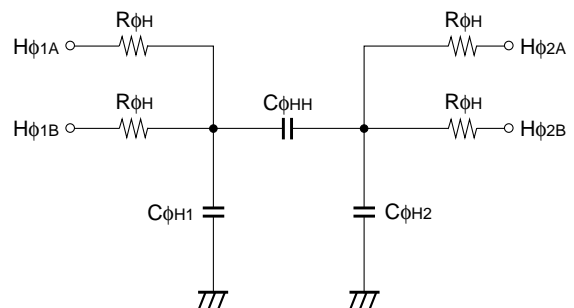
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform Diagram	Remarks
Readout clock voltage	V <sub>VT</sub>	14.55	15.0	15.45	V	1	
Vertical transfer clock voltage	V <sub>VH1</sub> , V <sub>VH2</sub> V <sub>VH3</sub> , V <sub>VH4</sub>	-0.05	0	0.05	V	2	$V_{VH} = (V_{VH1} + V_{VH2} + V_{VH3} + V_{VH4})/4$
	V <sub>VH5</sub> , V <sub>VH6</sub>	-0.2	0	0.05	V	2	
	V <sub>VL1</sub> , V <sub>VL2</sub> , V <sub>VL3</sub> , V <sub>VL4</sub> , V <sub>VL5</sub> , V <sub>VL6</sub>	-8.0	-7.5	-7.0	V	2	$V_{VL} = (V_{VL5} + V_{VL6})/2$
	V <sub>φV</sub>	6.8	7.5	8.05	V	2	$V_{φV} = V_{VHn} - V_{VLn} (n = 1 \text{ to } 6)$
	V <sub>VH5</sub> - V <sub>VH</sub>	-0.25		0.1	V	2	
	V <sub>VH6</sub> - V <sub>VH</sub>	-0.25		0.1	V	2	
	V <sub>VHH</sub>			0.8	V	2	High-level coupling
	V <sub>VHL</sub>			0.9	V	2	High-level coupling
	V <sub>VLH</sub>			0.9	V	2	Low-level coupling
	V <sub>VLL</sub>			0.8	V	2	Low-level coupling
Horizontal transfer clock voltage	V <sub>φH</sub>	3.0	3.3	3.6	V	3	
	V <sub>H</sub> L	-0.05	0	0.05	V	3	
	V <sub>CR</sub>	V <sub>φH</sub> /2			V	3	Cross-point voltage
Reset gate clock voltage	V <sub>φRG</sub>	3.0	3.3	3.6	V	4	
	V <sub>RGLH</sub> - V <sub>RGLL</sub>			0.4	V	4	Low-level coupling
	V <sub>RGL</sub> - V <sub>RGLm</sub>			0.5	V	4	Low-level coupling
Substrate clock voltage	V <sub>φSUB</sub>	21.5	22.5	23.5	V	5	

**Clock Equivalent Circuit Constants** (Estimated values for horizontal transfer clock and reset gate clock)

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C\phi V1$		4700		pF	
	$C\phi V2, C\phi V4, C\phi V6$		3300		pF	
	$C\phi V3A$		1800		pF	
	$C\phi V3B$		3300		pF	
	$C\phi V5A$		1800		pF	
	$C\phi V5B$		2200		pF	
Capacitance between vertical transfer clocks	$C\phi V12$		470		pF	
	$C\phi V23A, C\phi V23B, C\phi V45A, C\phi V45B$		47		pF	
	$C\phi V3A4, C\phi V3B4, C\phi V5A6, C\phi V5B6$		270		pF	
	$C\phi V61$		100		pF	
Capacitance between horizontal transfer clock and GND	$C\phi H1, C\phi H2$		33		pF	
Capacitance between horizontal transfer clocks	$C\phi HH$		120		pF	
Capacitance between reset gate clock and GND	$C\phi RG$		6		pF	
Capacitance between substrate clock and GND	$C\phi SUB$		820		pF	
Vertical transfer clock series resistor	$R1, R2, R4, R5B, R6$		180		$\Omega$	
	$R3A$		330		$\Omega$	
	$R3B$		240		$\Omega$	
	$R5A$		490		$\Omega$	
Vertical transfer clock ground resistor	$R_{GND}$		18		$\Omega$	
Horizontal transfer clock series resistor	$R\phi H$		7.5		$\Omega$	



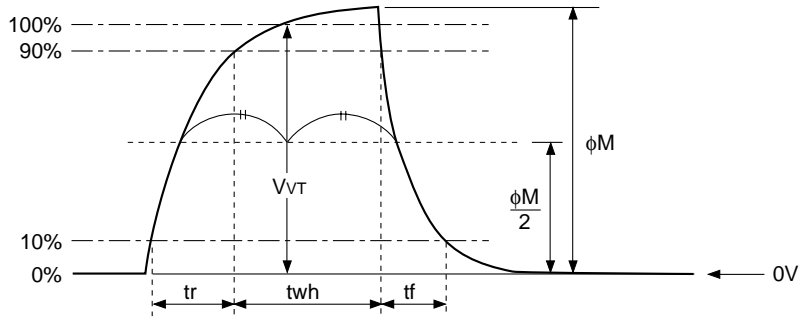
**Vertical transfer clock equivalent circuit**



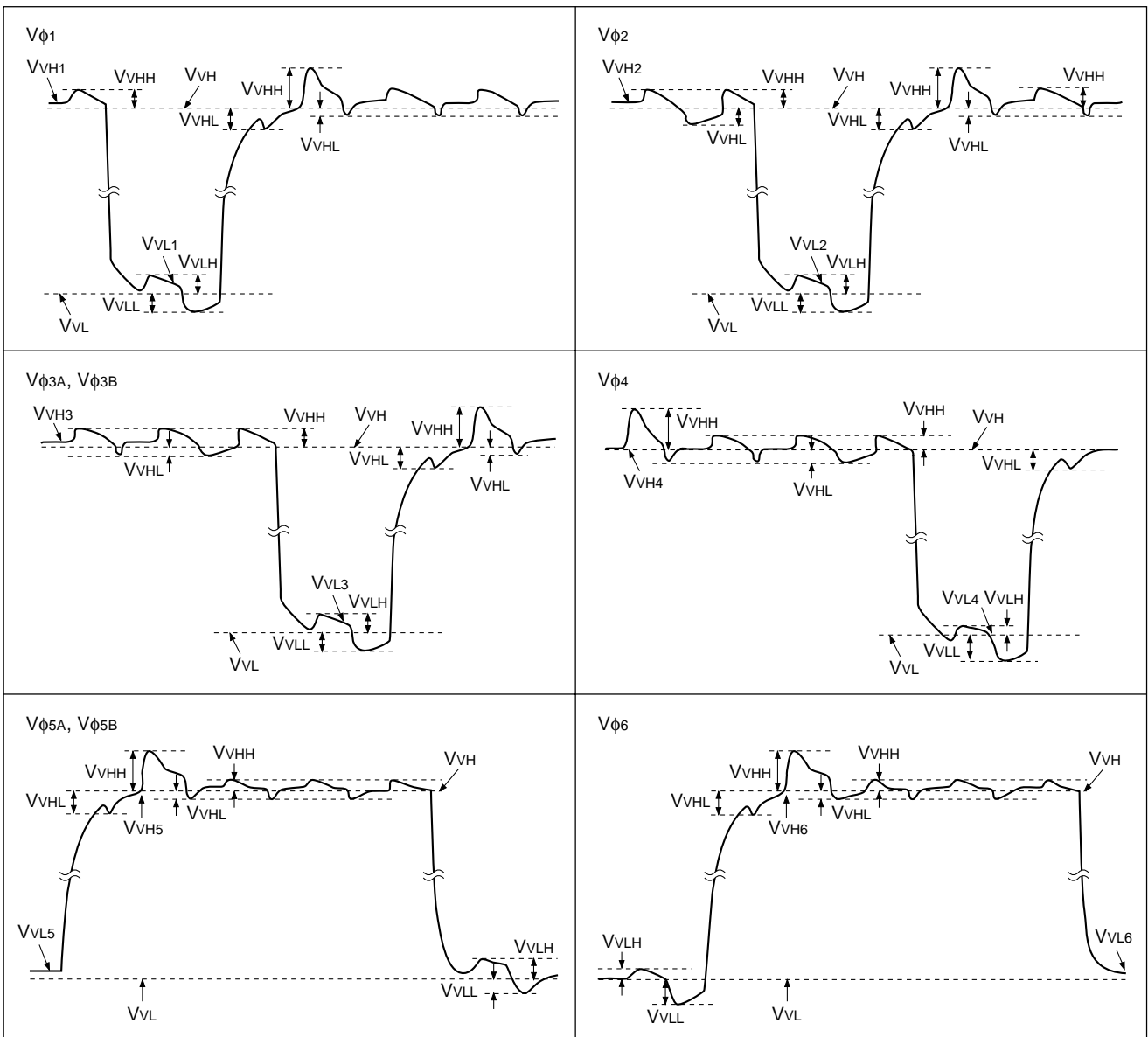
**Horizontal transfer clock equivalent circuit**

Drive Clock Waveform Conditions

(1) Readout clock waveform



(2) Vertical transfer clock waveform

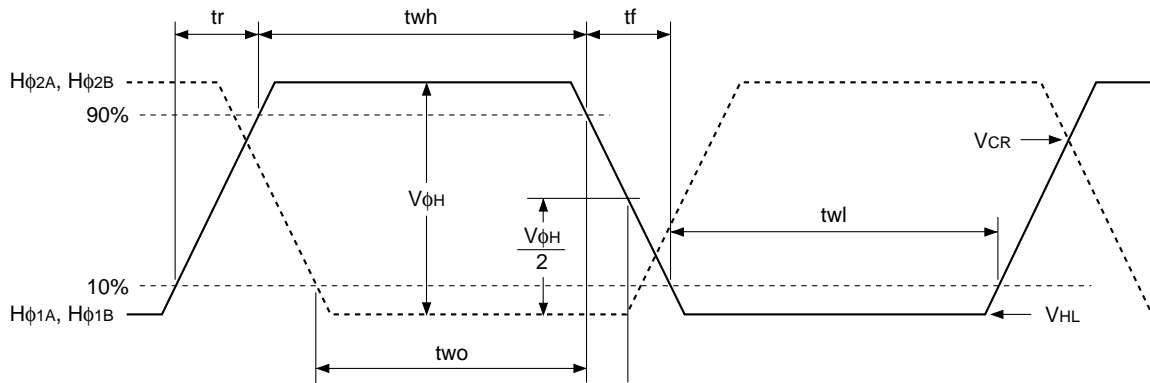


$$V_{VH} = (V_{VH1} + V_{VH2} + V_{VH3} + V_{VH4})/4$$

$$V_{VL} = (V_{VL5} + V_{VL6})/2$$

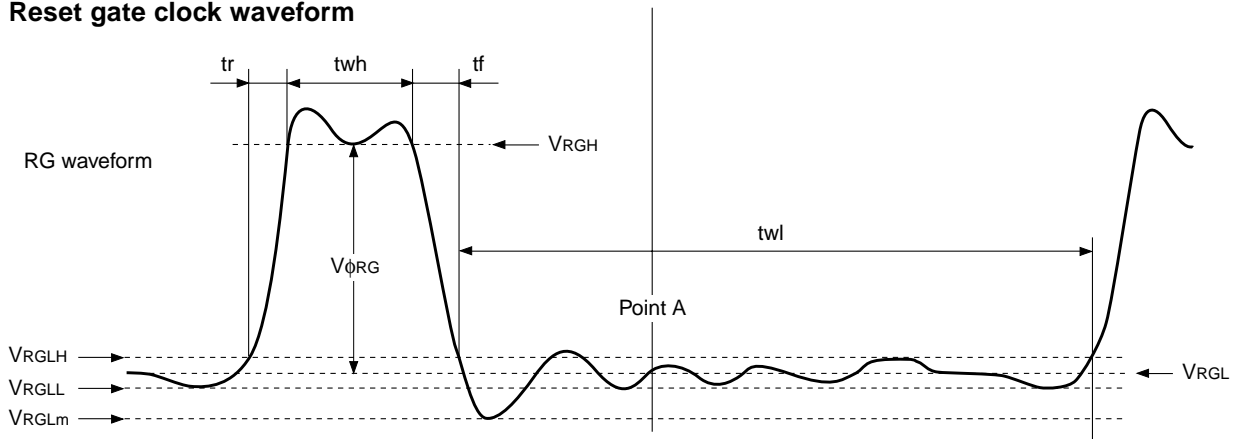
$$V_{\phi n} = V_{VHn} - V_{VLn} \quad (n = 1 \text{ to } 6)$$

**(3) Horizontal transfer clock waveform**



Cross-point voltage for the Hφ<sub>1</sub> rising side of the horizontal transfer clocks Hφ<sub>1</sub> and Hφ<sub>2</sub> waveforms is V<sub>CR</sub>. The overlap period for t<sub>wh</sub> and t<sub>wl</sub> of horizontal transfer clocks Hφ<sub>1</sub> and Hφ<sub>2</sub> is two.

**(4) Reset gate clock waveform**



V<sub>RGLH</sub> is the maximum value and V<sub>RGLL</sub> is the minimum value of the coupling waveform during the period from Point A in the above diagram until the rising edge of RG.

In addition, V<sub>RGL</sub> is the average value of V<sub>RGLH</sub> and V<sub>RGLL</sub>.

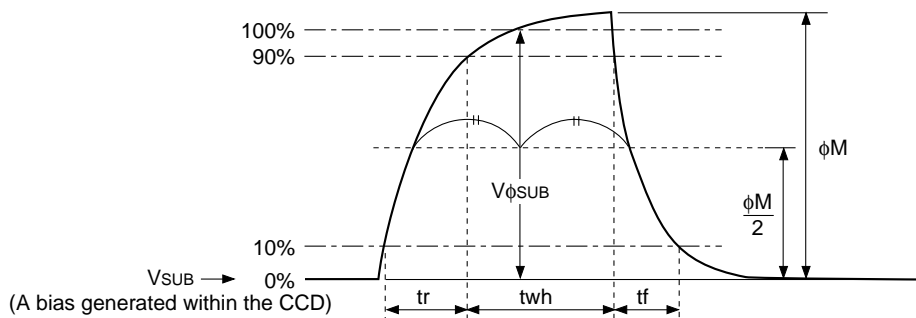
$$V_{RGL} = (V_{RGLH} + V_{RGLL})/2$$

Assuming V<sub>RGH</sub> is the minimum value during the interval with t<sub>wh</sub>, then:

$$V_{\phi RG} = V_{RGH} - V_{RGL}$$

Negative overshoot level during the falling edge of RG is V<sub>RGLm</sub>.

**(5) Substrate clock waveform**



**Clock Switching Characteristics** (Horizontal drive frequency: 24.3MHz)

Item	Symbol	twh			twl			tr			tf			Unit	Remarks
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Readout clock	V <sub>T</sub>	3.18	3.42						0.5			0.5		μs	During readout
Vertical transfer clock	V <sub>φ1</sub> , V <sub>φ2</sub> , V <sub>φ3A</sub> , V <sub>φ3B</sub> , V <sub>φ4</sub> , V <sub>φ5A</sub> , V <sub>φ5B</sub> , V <sub>φ6</sub>										15		350	ns	When using CXD3400N
Horizontal transfer clock	H <sub>φ1</sub>	11	15		11	15			6.0	9.5		6.0	9.5	ns	tf ≥ tr – 2ns
	H <sub>φ2</sub>	11	15		11	15			6.0	9.5		6.0	9.5		
Reset gate clock	φ <sub>RG</sub>	6	8			28			3			3		ns	
Substrate clock	φ <sub>SUB</sub>	2.5	3.02							0.5			0.5	μs	During drain charge

Item	Symbol	two			Unit	Remarks
		Min.	Typ.	Max.		
Horizontal transfer clock	H <sub>φ1A</sub> , H <sub>φ1B</sub> , H <sub>φ2A</sub> , H <sub>φ2B</sub>	10	15		ns	*1

\*1 The overlap period for twh and twl of horizontal transfer clocks H<sub>φ1</sub> and H<sub>φ2</sub> is two.

**Spectral Sensitivity Characteristics** (excludes lens characteristics and light source characteristics)

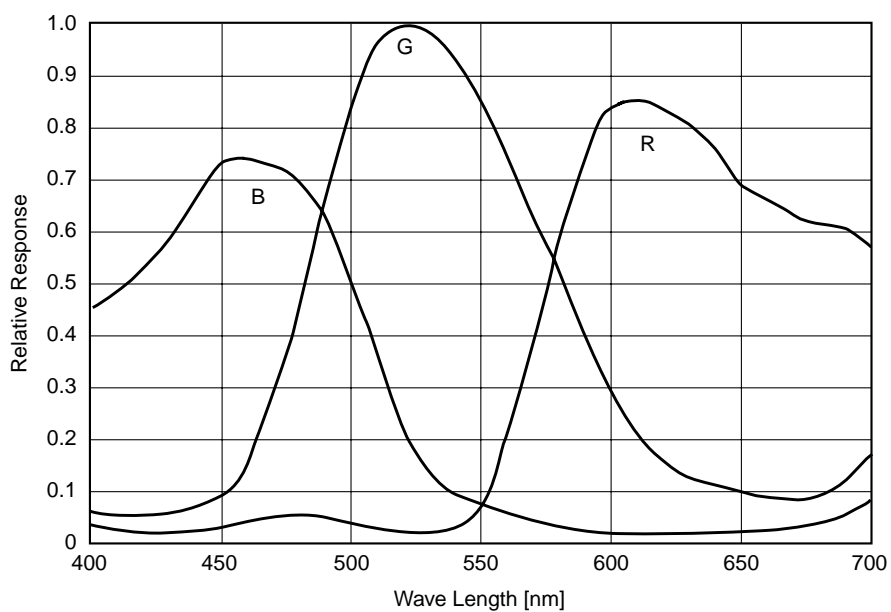




Image Sensor Characteristics (horizontal drive frequency: 24.3MHz)

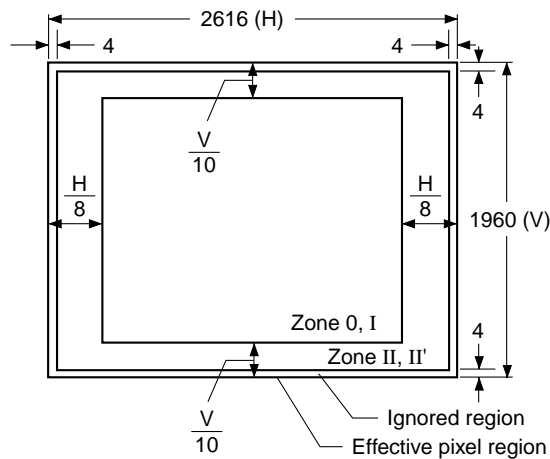
(Ta = 25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks
G Sensitivity	Sg	195	260	325	mV	1	1/30s accumulation
Sensitivity comparison	R	Rr	0.41	0.67		1	
	B	Rb	0.30	0.57		1	
Saturation signal	Vsat	500			mV	2	Ta = 60°C
Smear	Sm		-90	-80	dB	3	Frame readout mode*1
			-77	-67			High frame rate readout mode
Video signal shading	SHg			20	%	4	Zone 0 and I
				25			Zone 0 to II'
Dark signal	Vdt			16	mV	5	Ta = 60°C, 3.75 frame/s
Dark signal shading	$\Delta Vdt$			8	mV	6	Ta = 60°C, 3.75 frame/s, *2
Line crawl G	Lcg			3.8	%	7	
Line crawl R	Lcr			3.8	%	7	
Line crawl B	Lcb			3.8	%	7	
Lag	Lag			0.5	%	8	

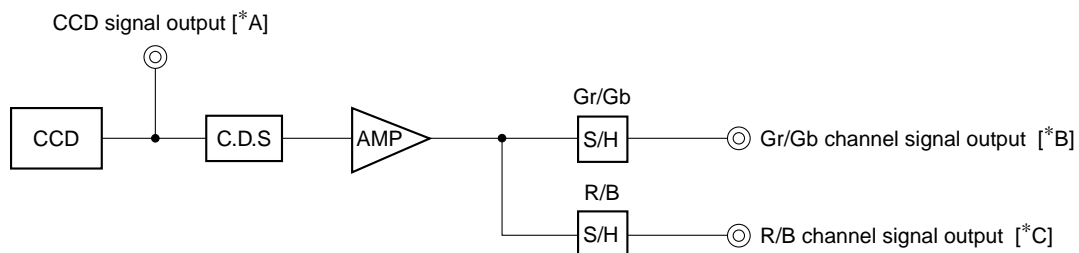
\*1 After closing the mechanical shutter, the smear can be reduced to below the detection limit by performing vertical register sweep operation.

\*2 Excludes vertical dark signal shading caused by vertical register high-speed transfer.

Zone Definition of Video Signal Shading



Measurement System



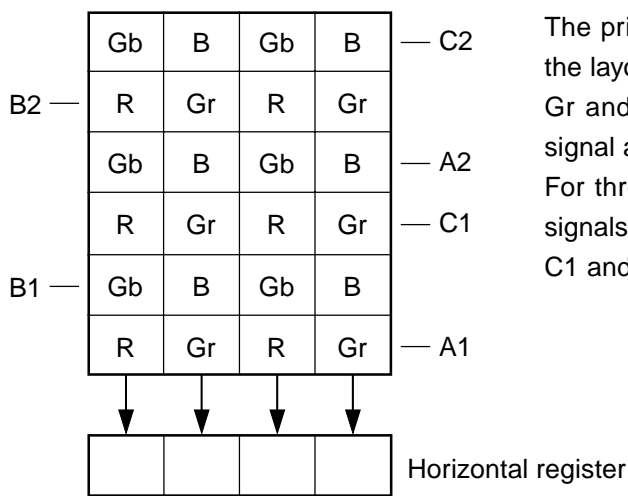
Note) Adjust the amplifier gain so that the gain between [\*A] and [\*B], and between [\*A] and [\*C] equals 1.

**Image Sensor Characteristics Measurement Method**

◎ **Measurement conditions**

- (1) In the following measurements, the device drive conditions are at the typical values of the bias and clock voltage conditions, and the frame readout mode is used. In addition,  $V_{SUB}$  Cont. is turned off.
- (2) In the following measurements, spot blemishes are excluded and, unless otherwise specified, the optical black level (OB) is used as the reference for the signal output, which is taken as the value of the Gr/Gb channel signal output or the R/B channel signal output of the measurement system.

◎ **Color coding of this image sensor & Readout**



The primary color filters of this image sensor are arranged in the layout shown in the figure on the left (Bayer arrangement). Gr and Gb denote the G signals on the same line as the R signal and the B signal, respectively. For three frames readout, the A1 and A2 lines are output as signals in the A field, the B1 and B2 lines in the B field, and the C1 and C2 lines in the C field.

**Color Coding Diagram**

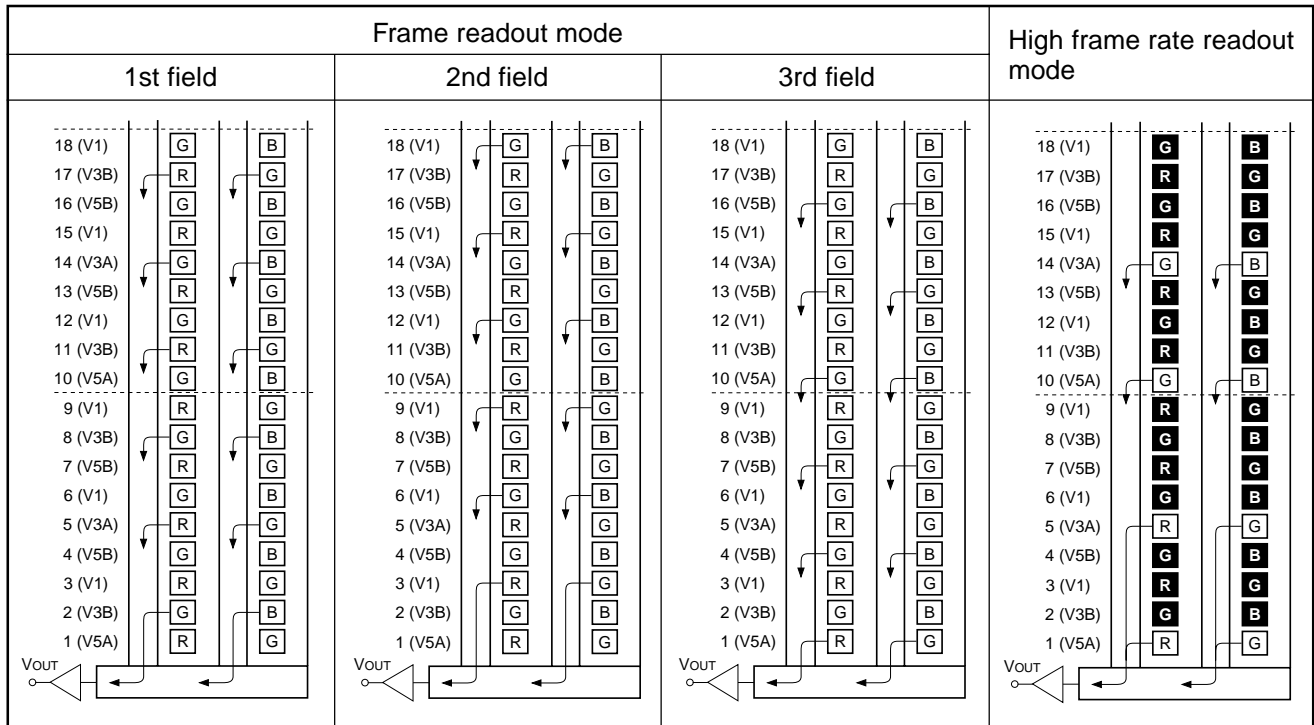
© Readout modes

1. Readout modes list

The following readout modes are possible by driving the image sensor at the timing specifications noted in this Data Sheet.

Mode name		Frame rate	Number of effective output lines
Frame readout mode	NTSC mode	3.75 frame/s	1960 (1st 653, 2nd 653, 3rd 654)
	PAL mode	3.57 frame/s	1960 (1st 653, 2nd 653, 3rd 654)
High frame rate readout mode	NTSC mode	30 frame/s	218
	PAL mode	25 frame/s	218
AF mode	NTSC mode	60 frame/s	66
	PAL mode	50 frame/s	66

2. Frame readout mode, high frame rate readout mode



**Note)** Blacked out portions in the diagram indicate pixels which are not read out.

1. Frame readout mode

In this mode, all pixel signals are divided into three fields and output.

All pixel signals are read out independently, making this mode suitable for high resolution image capturing.

2. High frame rate readout mode

Output is performed at 30 frames per second by reading out 4 pixels for every 18 vertical pixels and adding 2 pixels in the horizontal CCD.

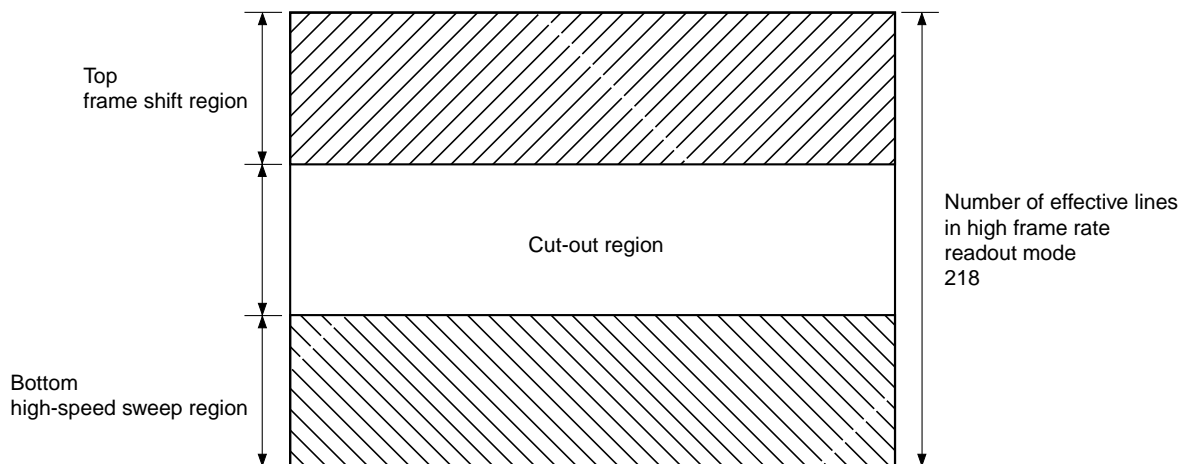
The number of output lines is 218 lines.

This readout mode emphasizes processing speed over vertical resolution.

### 3. AF mode

The AF mode increases the frame rate by cutting out a portion of the picture through high-speed elimination of the top and bottom of the picture in 4/18 line readout mode. This mode allows 1/60s and 1/50s output, so it is effective for raising the auto focus (AF) speed.

In addition, the cut-out start position can be selected. See the timing specifications for details.



## ◎ Definition of standard imaging conditions

### (1) Standard imaging condition I:

Use a pattern box (luminance: 706cd/m<sup>2</sup>, color temperature of 3200K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter and image at F5.6. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

### (2) Standard imaging condition II:

Image a light source (color temperature of 3200K) with a uniformity of brightness within 2% at all angles. Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

### (3) Standard imaging condition III:

Image a light source (color temperature of 3200K) with a uniformity of brightness within 2% at all angles. Use a testing standard lens (exit pupil distance –33mm) with CM500S (t = 1.0mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

#### 1. G Sensitivity, sensitivity comparison

Set to the standard imaging condition I. After setting the electronic shutter mode with a shutter speed of 1/100s, measure the signal outputs ( $V_{Gr}$ ,  $V_{Gb}$ ,  $V_R$  and  $V_B$ ) at the center of each Gr, Gb, R and B channel screen, and substitute the values into the following formulas.

$$V_G = (V_{Gr} + V_{Gb})/2$$

$$S_g = V_G \times \frac{100}{30} \text{ [mV]}$$

$$R_r = V_R/V_G$$

$$R_b = V_B/V_G$$

#### 2. Saturation signal

Set to the standard imaging condition II. After adjusting the luminous intensity to 20 times the intensity with the average value of the Gr signal output, 150mV, measure the minimum values of the Gr, Gb, R and B signal outputs.

#### 3. Smear

Set to the standard imaging condition III. With the lens diaphragm at F5.6 to F8, first adjust the average value of the Gr signal output to 150mV. Measure the average values of the Gr signal output, Gb signal output, R signal output and B signal output ( $G_{ra}$ ,  $G_{ba}$ ,  $R_a$ ,  $B_a$ ), and then adjust the luminous intensity to 500 times the intensity with the average value of the Gr signal output, 150mV.

After the readout clock is stopped and the charge drain is executed by the electronic shutter at the respective H blankings, measure the maximum value ( $V_{sm}$  [mV]) independent of the Gr, Gb, R and B signal outputs, and substitute the values into the following formula.

The smear other than for the frame readout mode is calculated from the accumulation time and the signal addition system.

$$S_m = 20 \times \log \left( V_{sm} \div \frac{G_{ra} + G_{ba} + R_a + B_a}{4} \times \frac{1}{500} \times \frac{1}{10} \right) \text{ [dB]} \text{ (1/10V method conversion value)}$$

4. Video signal shading

Set to the standard imaging condition III. With the lens diaphragm at F5.6 to F8, adjusting the luminous intensity so that the average value of the Gr signal output is 150mV. Then measure the maximum value (Grmax [mV]) and minimum value (Grmin [mV]) of the Gr signal output and substitute the values into the following formula.

$$SHg = (Grmax - Grmin)/150 \times 100 \text{ [%]}$$

5. Dark signal

Measure the average value of the signal output (Vdt [mV]) with the device ambient temperature of 60°C and the device in the light-obstructed state, using the horizontal idle transfer level as a reference.

6. Dark signal shading

After measuring 5, measure the maximum (Vdmax [mV]) and minimum (Vdmin [mV]) values of the dark signal output and substitute the values into the following formula.

$$\Delta Vdt = Vdmax - Vdmin \text{ [mV]}$$

7. Line crawl

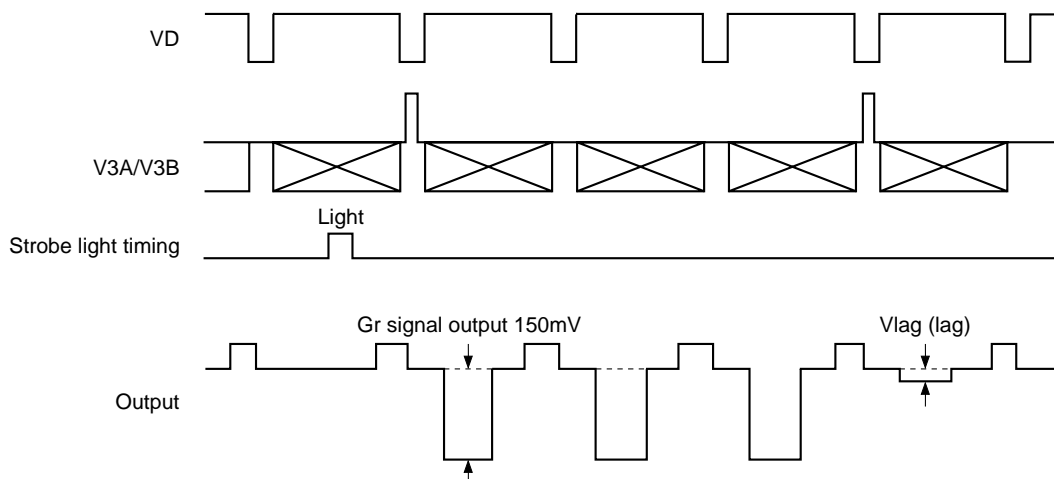
Set to the standard imaging condition II. Adjusting the luminous intensity so that the average value of the Gr signal output is 150mV, and then insert R, G and B filters and measure the difference between G signal lines ( $\Delta G_{lr}$ ,  $\Delta G_{lg}$ ,  $\Delta G_{lb}$  [mV]) as well as the average value of the G signal output ( $G_{ar}$ ,  $G_{ag}$ ,  $G_{ab}$ ). Substitute the values into the following formula.

$$Lci = \frac{\Delta G_{li}}{G_{ai}} \times 100 \text{ [%]} \text{ (i = r, g, b)}$$

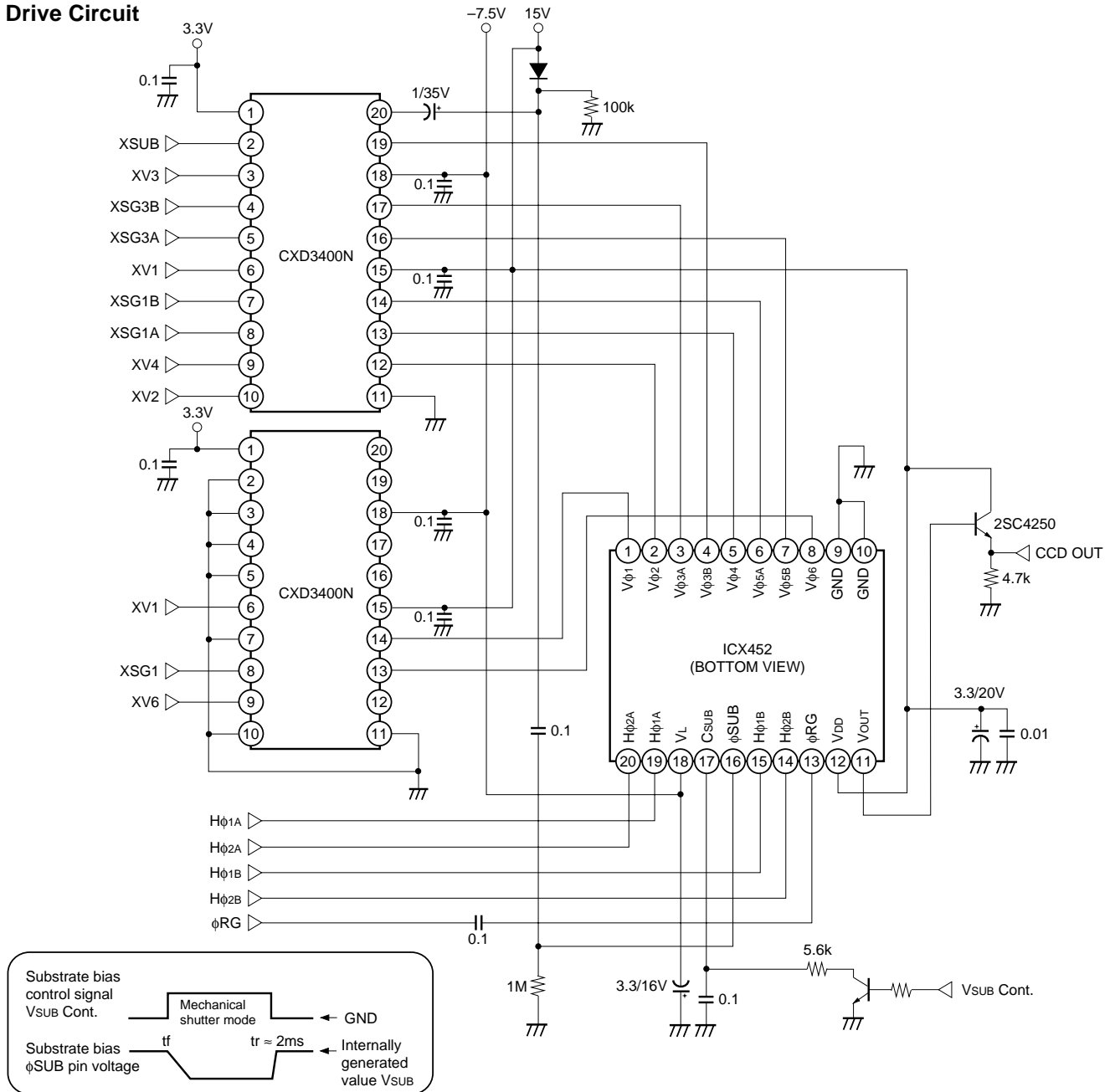
8. Lag

Adjust the Gr signal output value generated by the strobe light to 150mV. After setting the strobe light so that it strobesc with the following timing, measure the residual signal amount (Vlag). Substitute the value into the following formula.

$$Lag = (Vlag/150) \times 100 \text{ [%]}$$



Drive Circuit



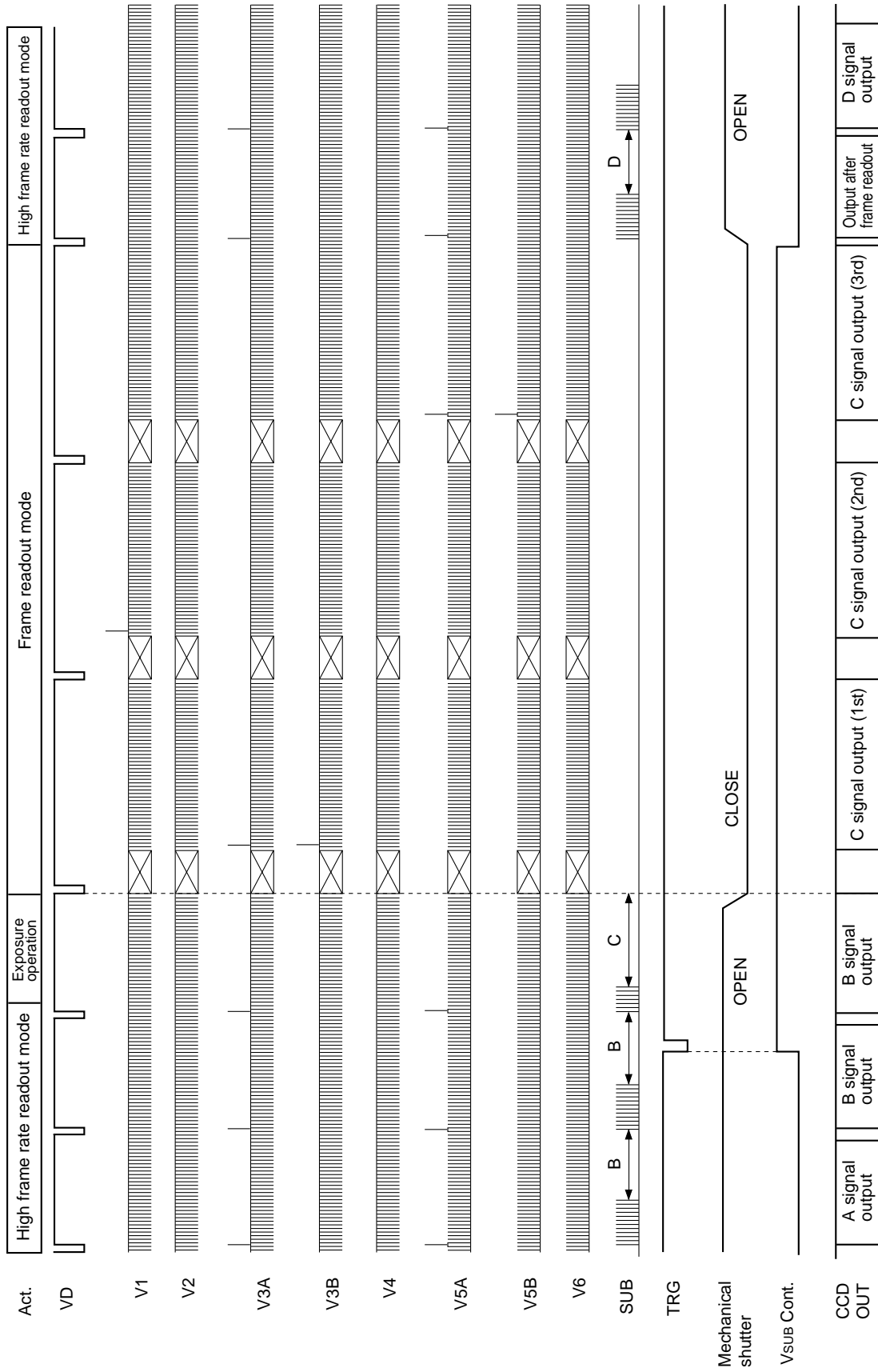
Notes) Substrate bias control

1. The saturation signal level decreases when exposure is performed using the mechanical shutter, so control the substrate bias.
2. A saturation signal level equivalent to that for continuous exposure can be assured by connecting a VR1 grounding resistor to the CCD CSUB pin.

Drive timing precautions

1. Blooming occurs in modes (high frame rate readout, etc.) that do not use the mechanical shutter, so do not ground the connected VR1 resistor.
2. tf is slow, so the internally generated voltage Vsub may not drop to a sufficiently low level if the substrate bias control signal is not set to high level 30ms before entering the exposure period and the VR1 resistor connected to the CSUB pin is not grounded.
3. The blooming signal generated during exposure in mechanical shutter mode is swept by providing one field or more (two fields recommended) of idle transfer through vertical register high-speed sweep transfer from the time the mechanical shutter closes until sensor readout is performed. However, note that the VL potential and the φSUB pin DC voltage sag at this time.

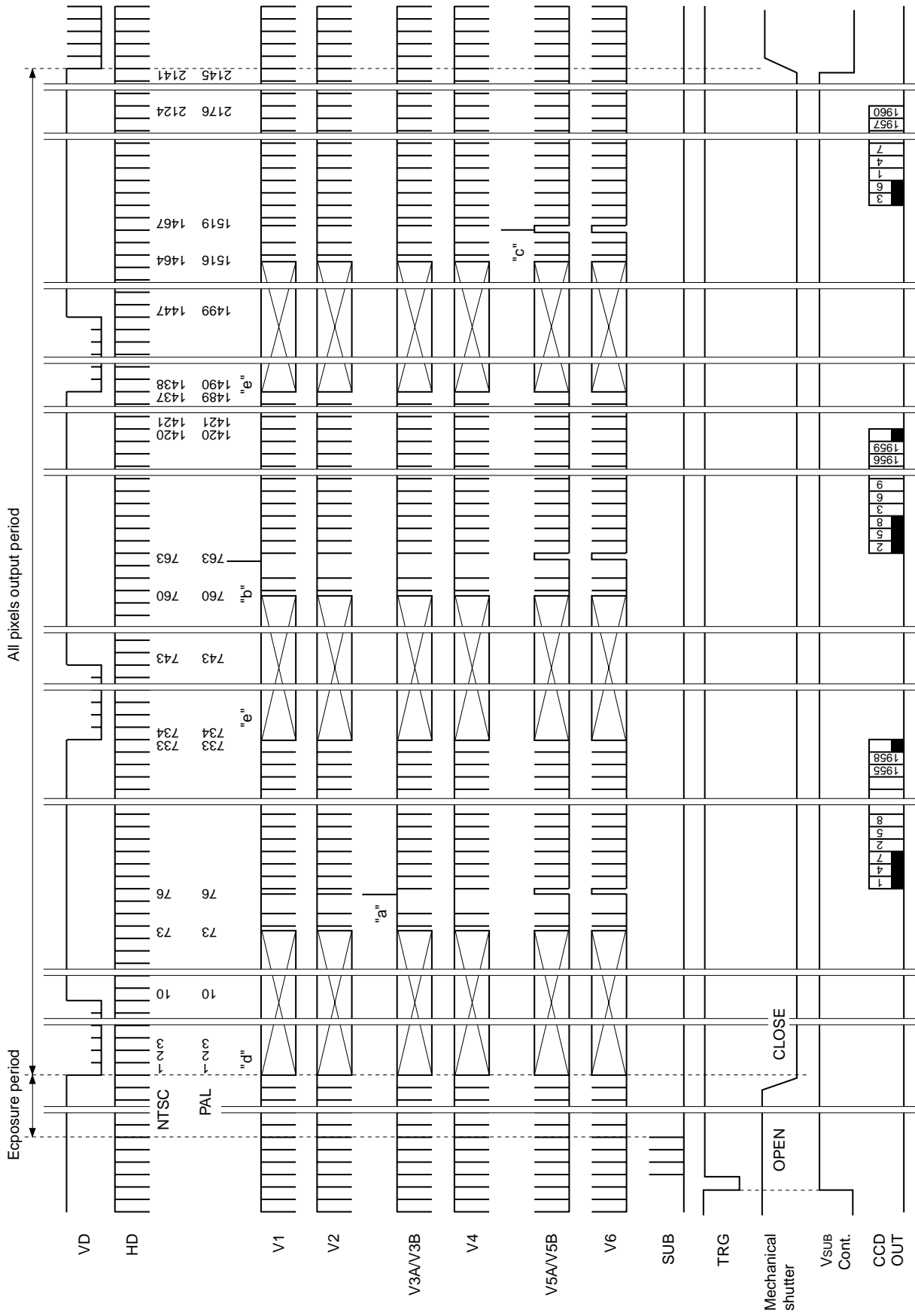
Drive Timing Chart (Vertical Sequence) High Frame Rate Readout Mode → Frame Readout Mode/Electronic Shutter Normal Operation



\* High frame rate readout mode out signals of V<sub>SUB</sub> Cont. high period contain a blooming component and should therefore not be used.  
 \* Apply 20 or more electronic shutter pulses at the start of exposure for the recording image.  
 If less than 20 pulses are applied, the electronic shutter may occur a discharge error.



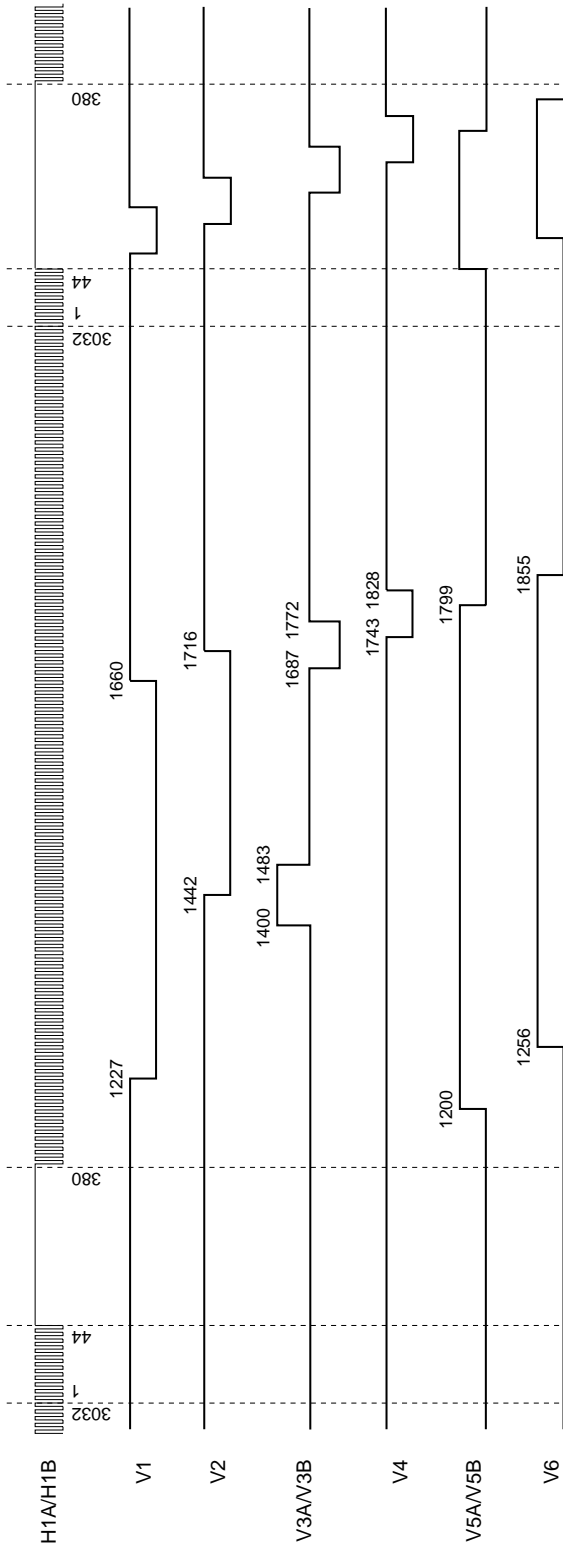
Drive Timing Chart (Vertical Sync) NTSC/PAL Frame Readout Mode



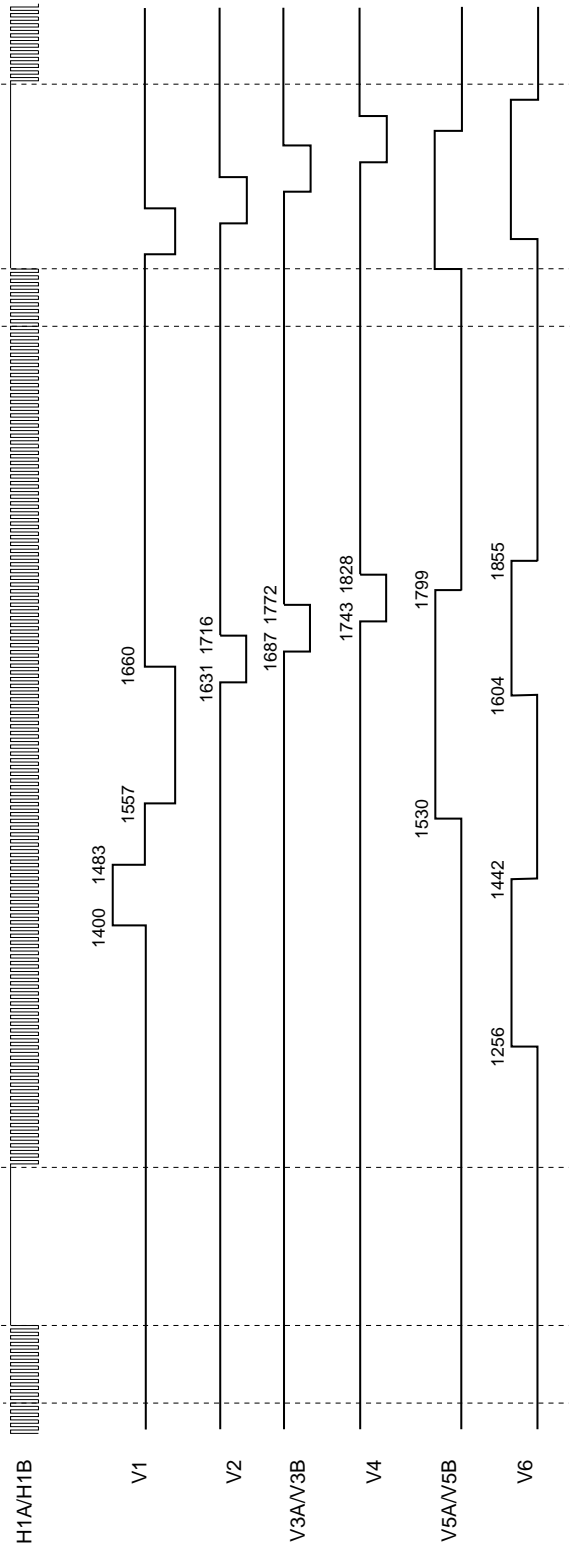
\* 3032H, however, 1437H and 2141H in NTSC mode are 516clk; 1489H and 2245H in PAL mode are 1612clk.

Drive Timing Chart (Vertical Sync) NTSC/PAL Frame Readout Mode

(Vertical Sync "a" Enlarged)

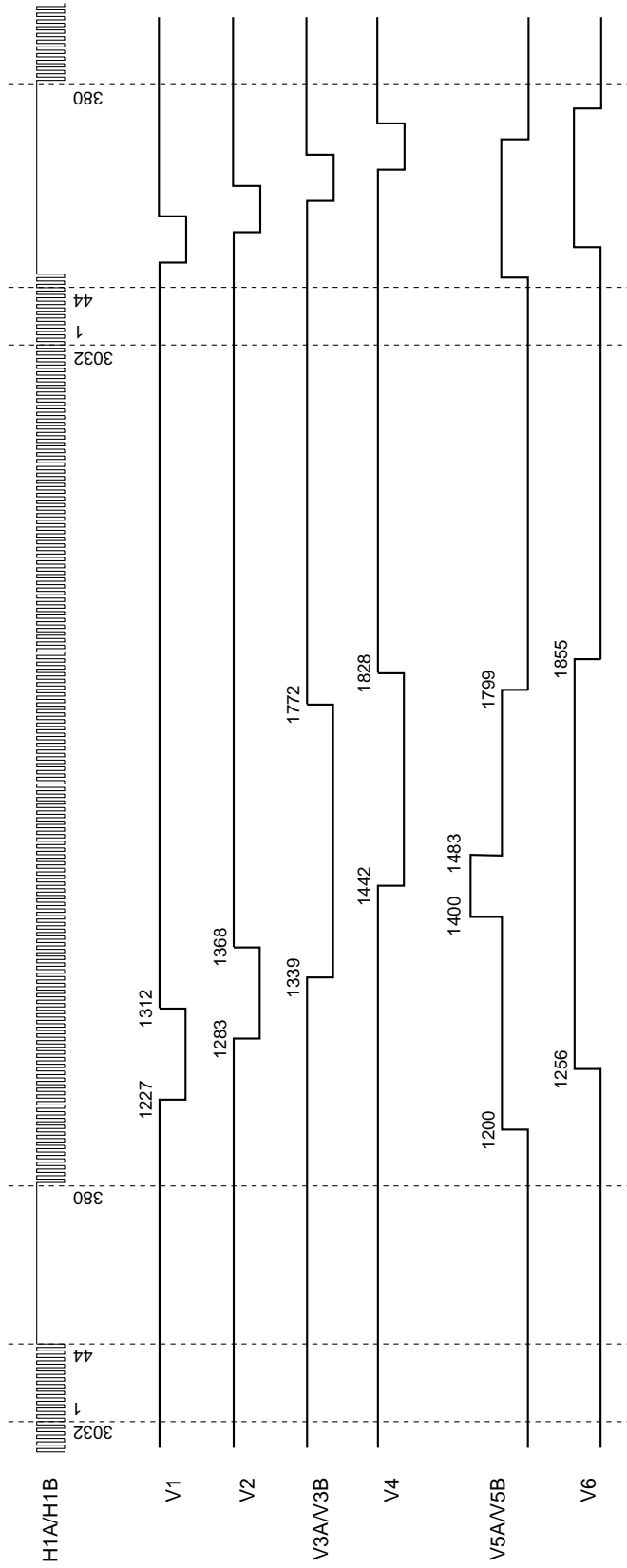


(Vertical Sync "b" Enlarged)



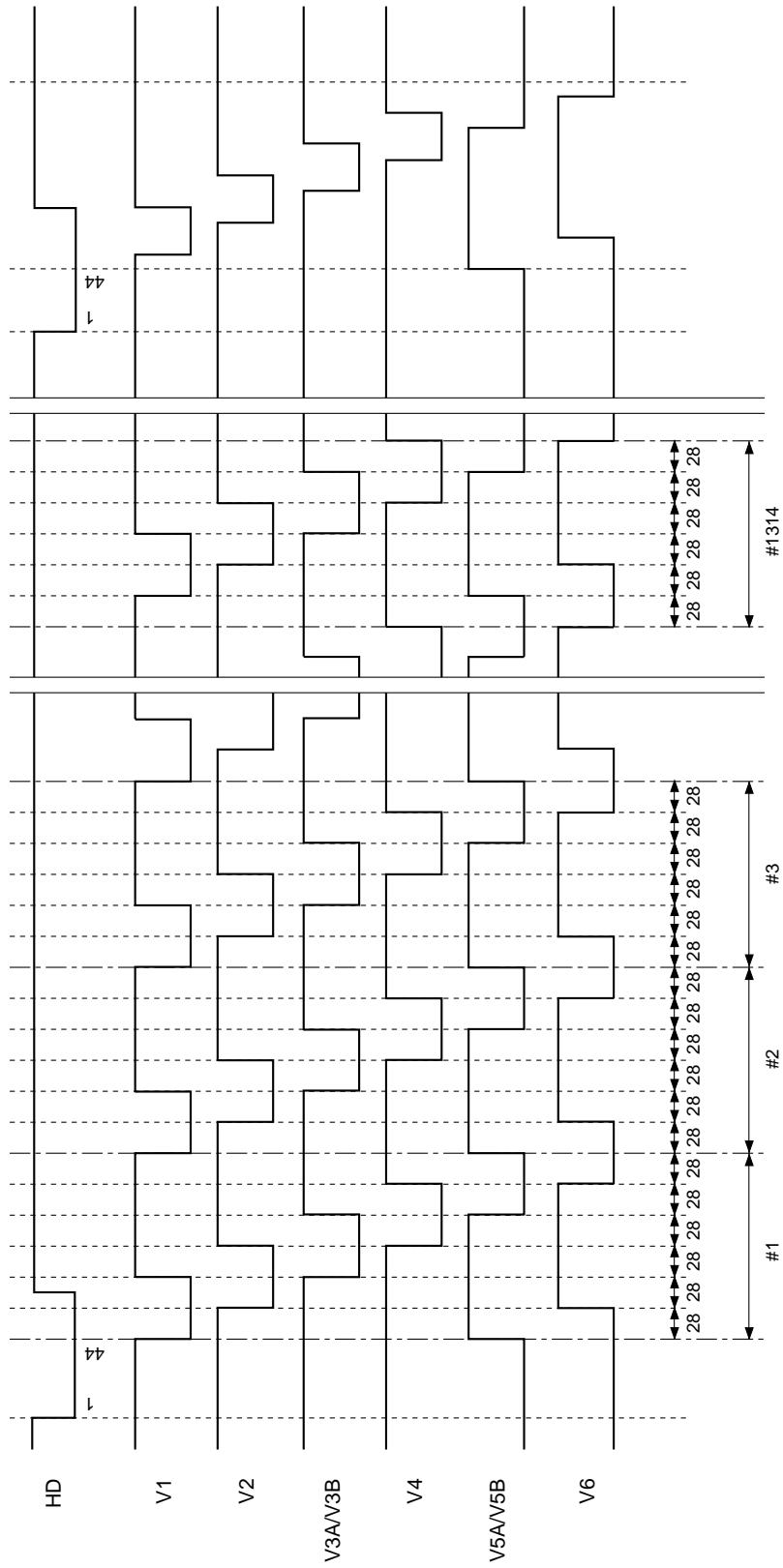
Drive Timing Chart (Vertical Sync) NTSC/PAL Frame Readout Mode

(Vertical Sync "c" Enlarged)



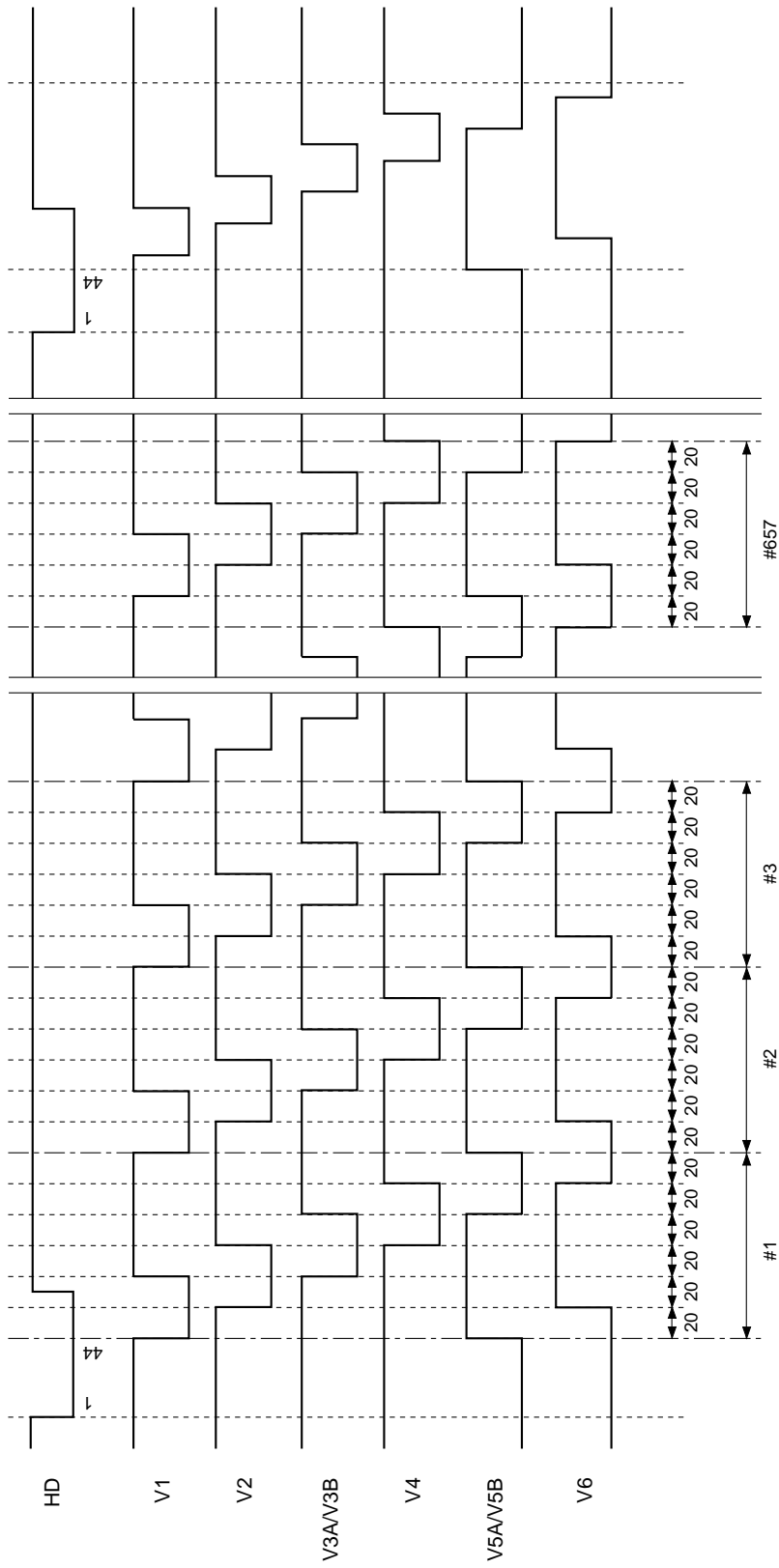
Drive Timing Chart (Vertical Sync) NTSC/PAL Frame Readout Mode

(Vertical Sync "d" Enlarged)

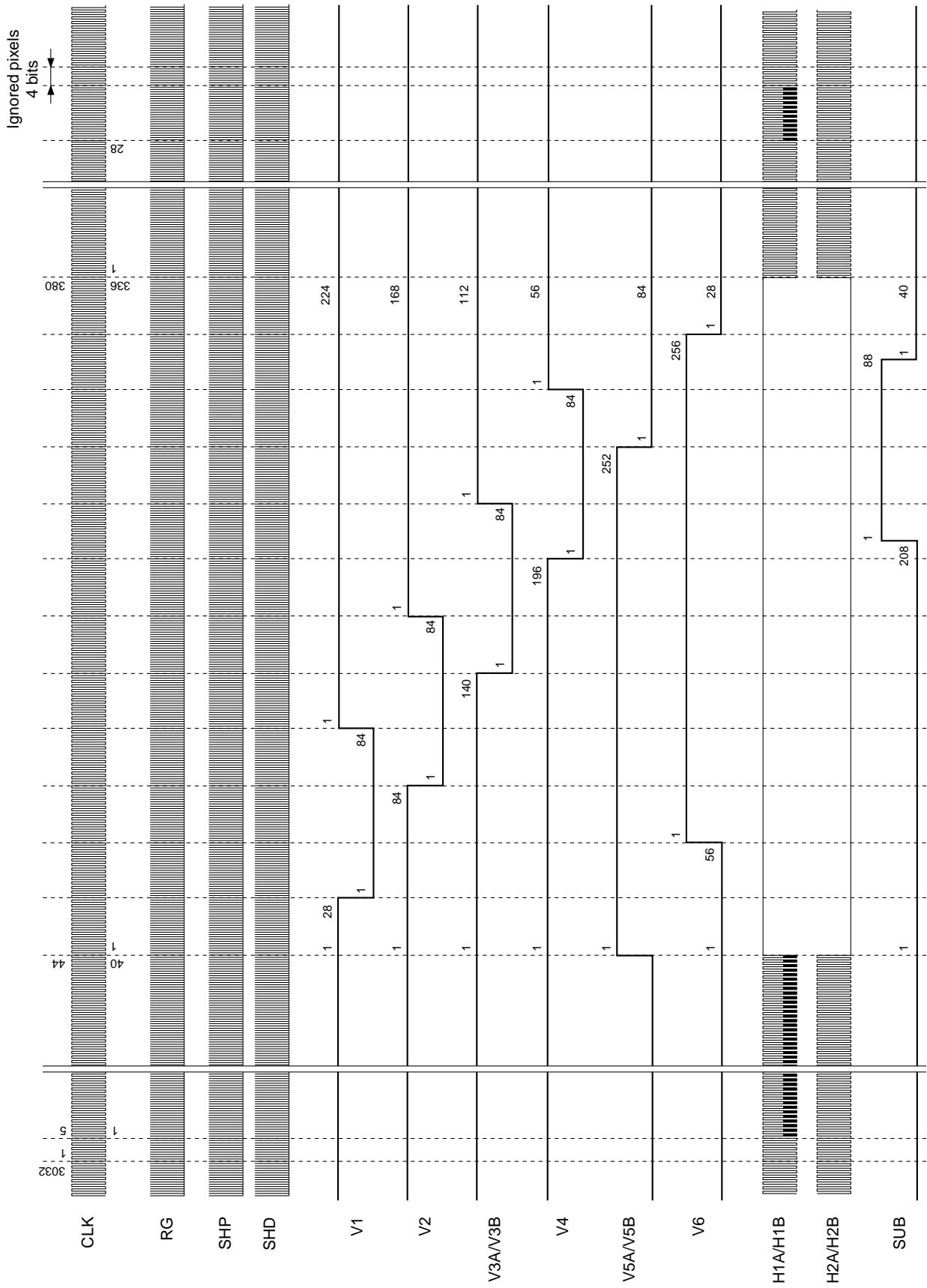


Drive Timing Chart (Vertical Sync)      NTSC/PAL      Frame Readout Mode

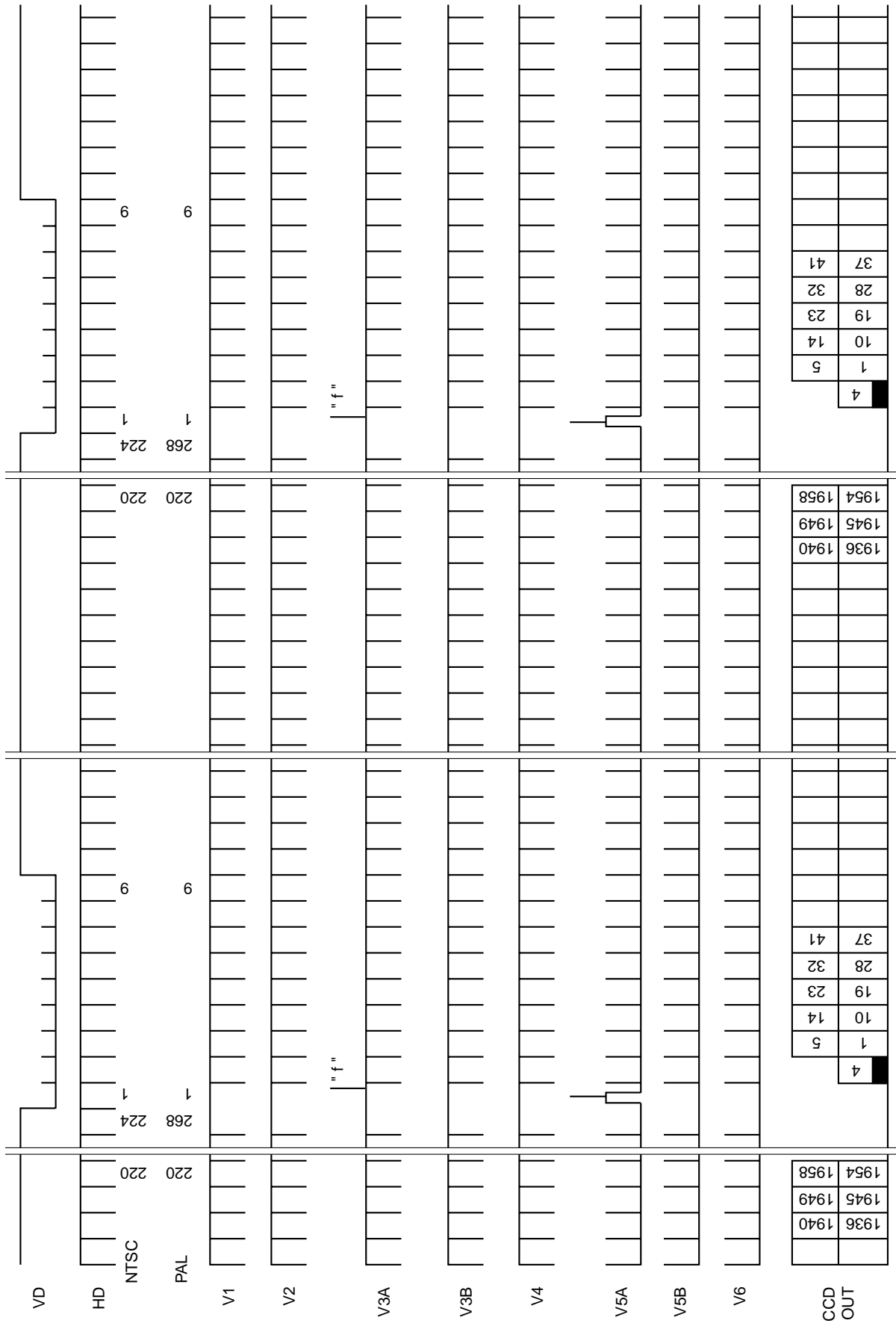
(Vertical Sync "e" Enlarged)



Drive Timing Chart (Horizontal Sync) NTSC/PAL Frame Readout Mode



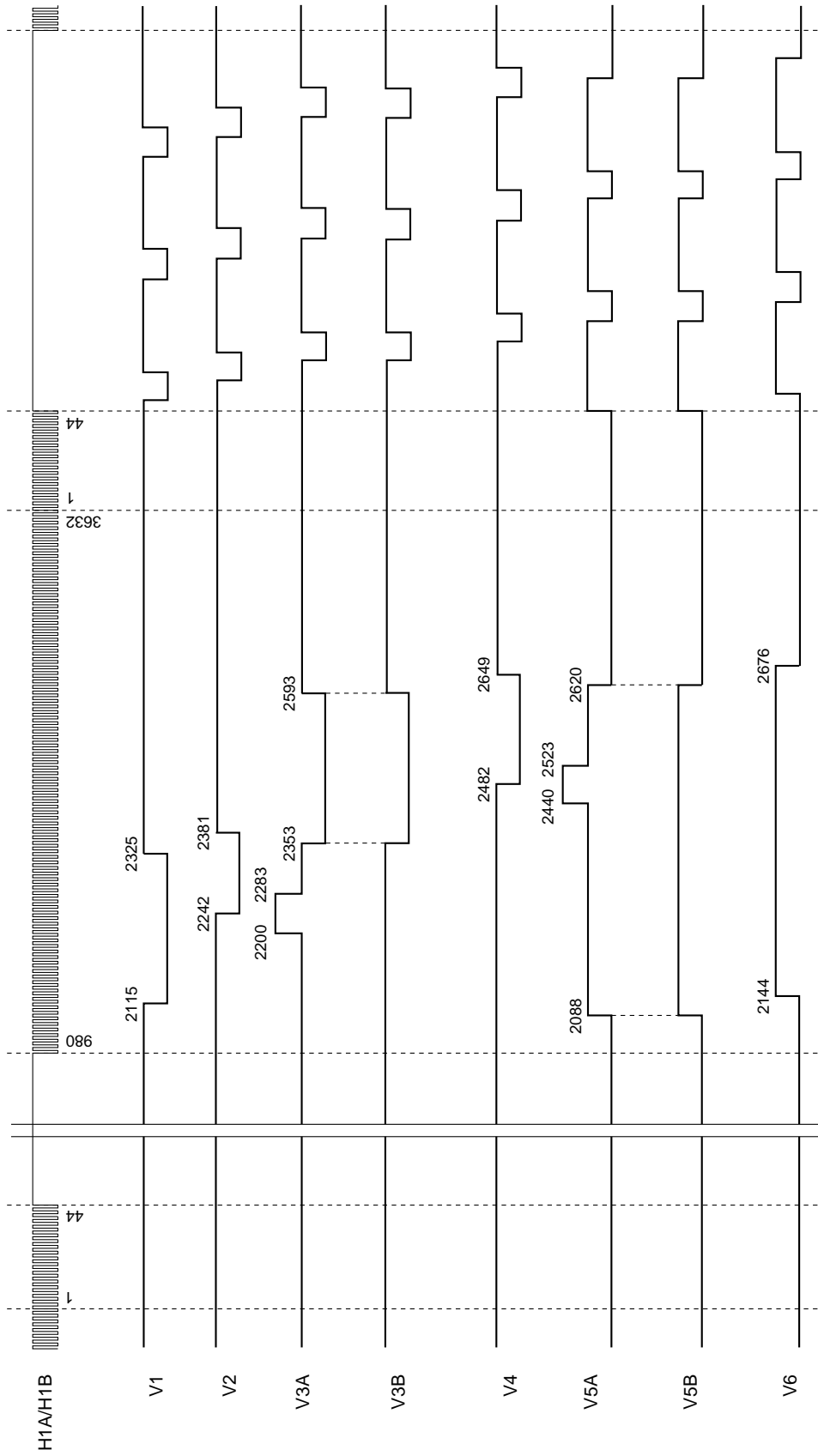
Drive Timing Chart (Vertical Sync) NTSC/PAL High Frame Rate Readout Mode



\* 3632H, however, 223H and 224H in NTSC mode are 2253clk; 268H in PAL mode is 2256clk.

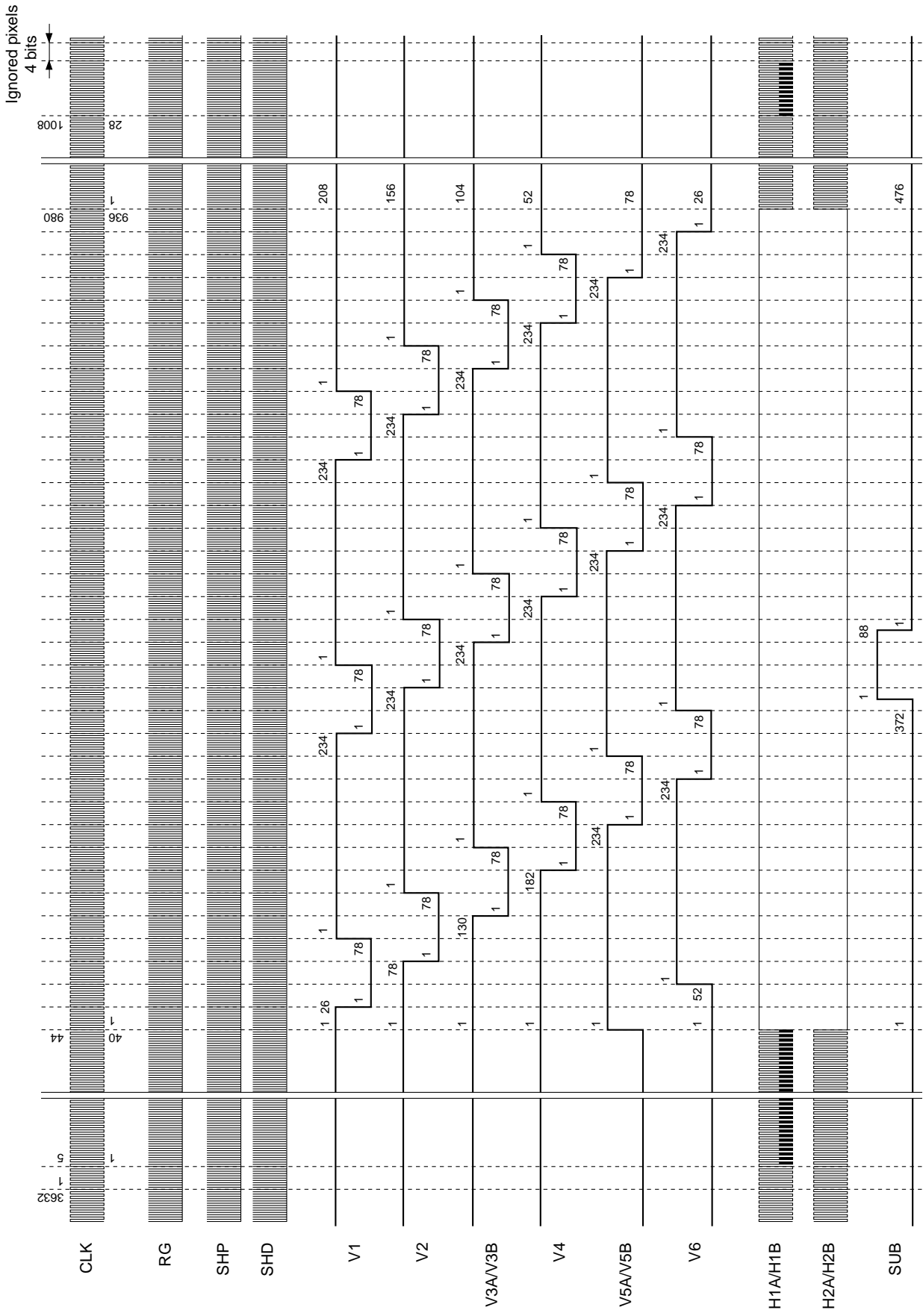
Drive Timing Chart (Vertical Sync) NTSC/PAL High Frame Rate Readout Mode

(Vertical Sync "f" Enlarged)

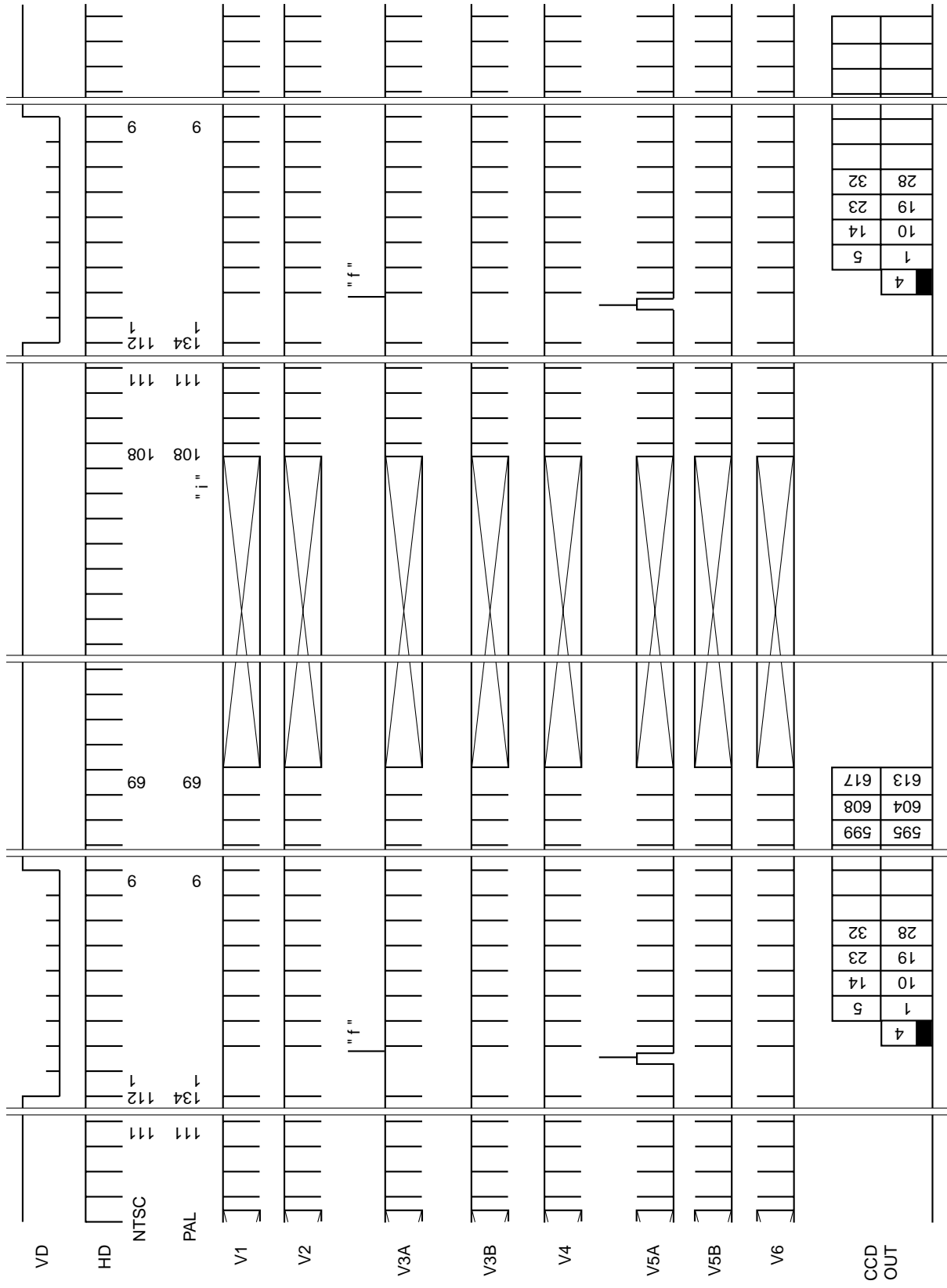




Drive Timing Chart (Horizontal Sync) NTSC/PAL High Frame Rate Readout Mode



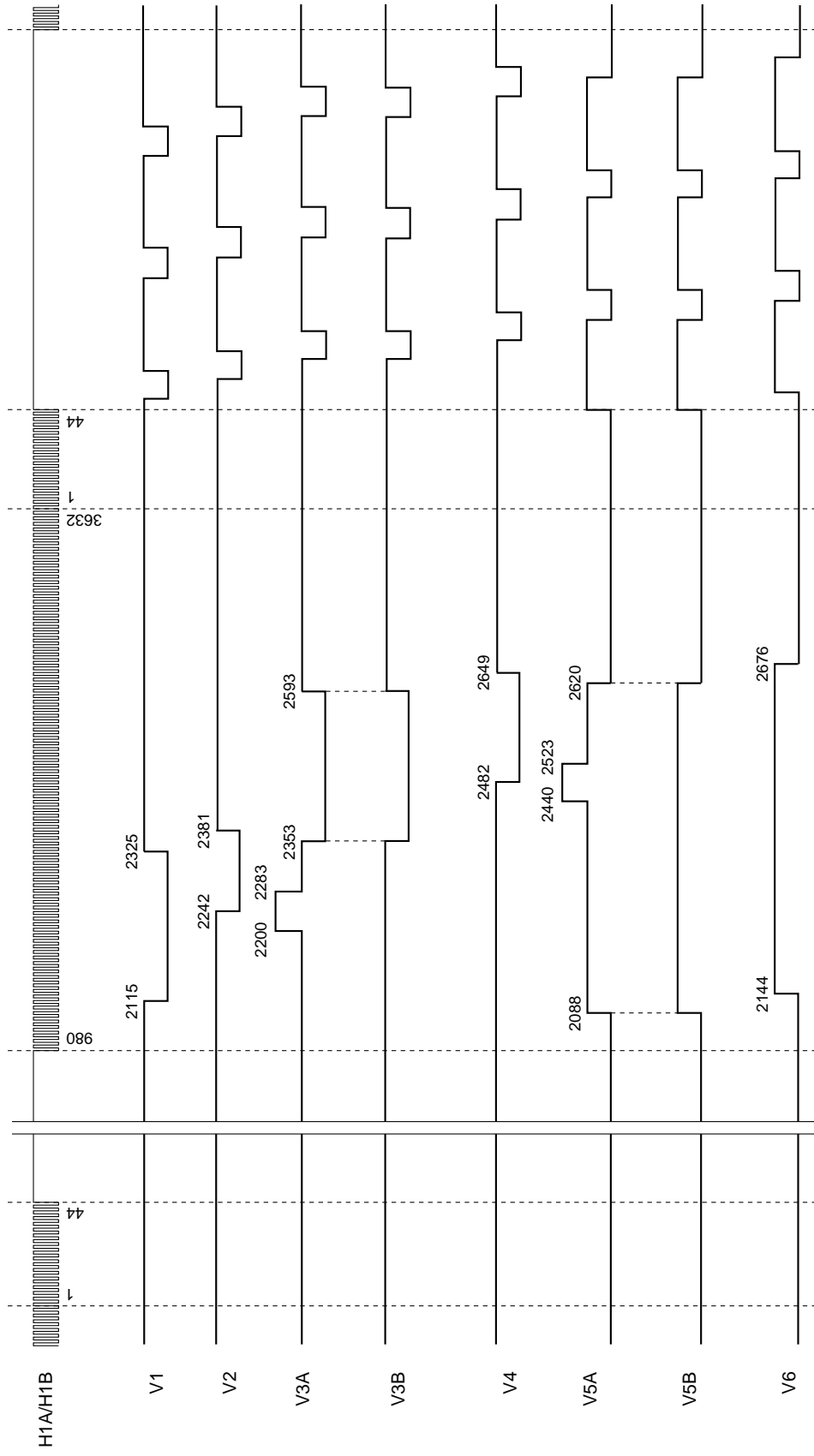
Drive Timing Chart (Vertical Sync) NTSC/PAL AF Mode (Upper)



\* 3632fH, however, 112H in NTSC mode is 2253clk; 134H in PAL mode is 2944clk.

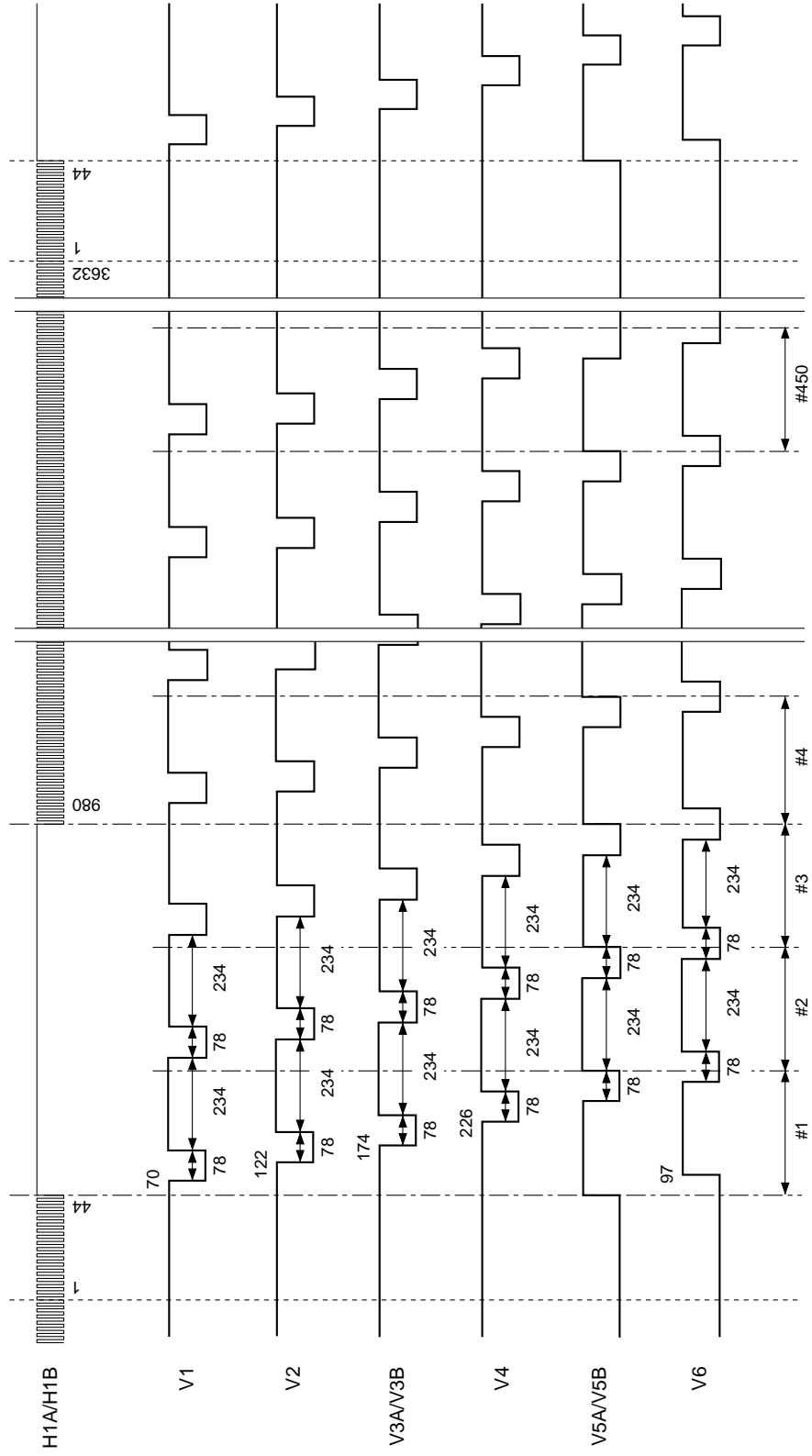
Drive Timing Chart (Vertical Sync) NTSC/PAL AF Mode (Upper)

(Vertical Sync "f" Enlarged)

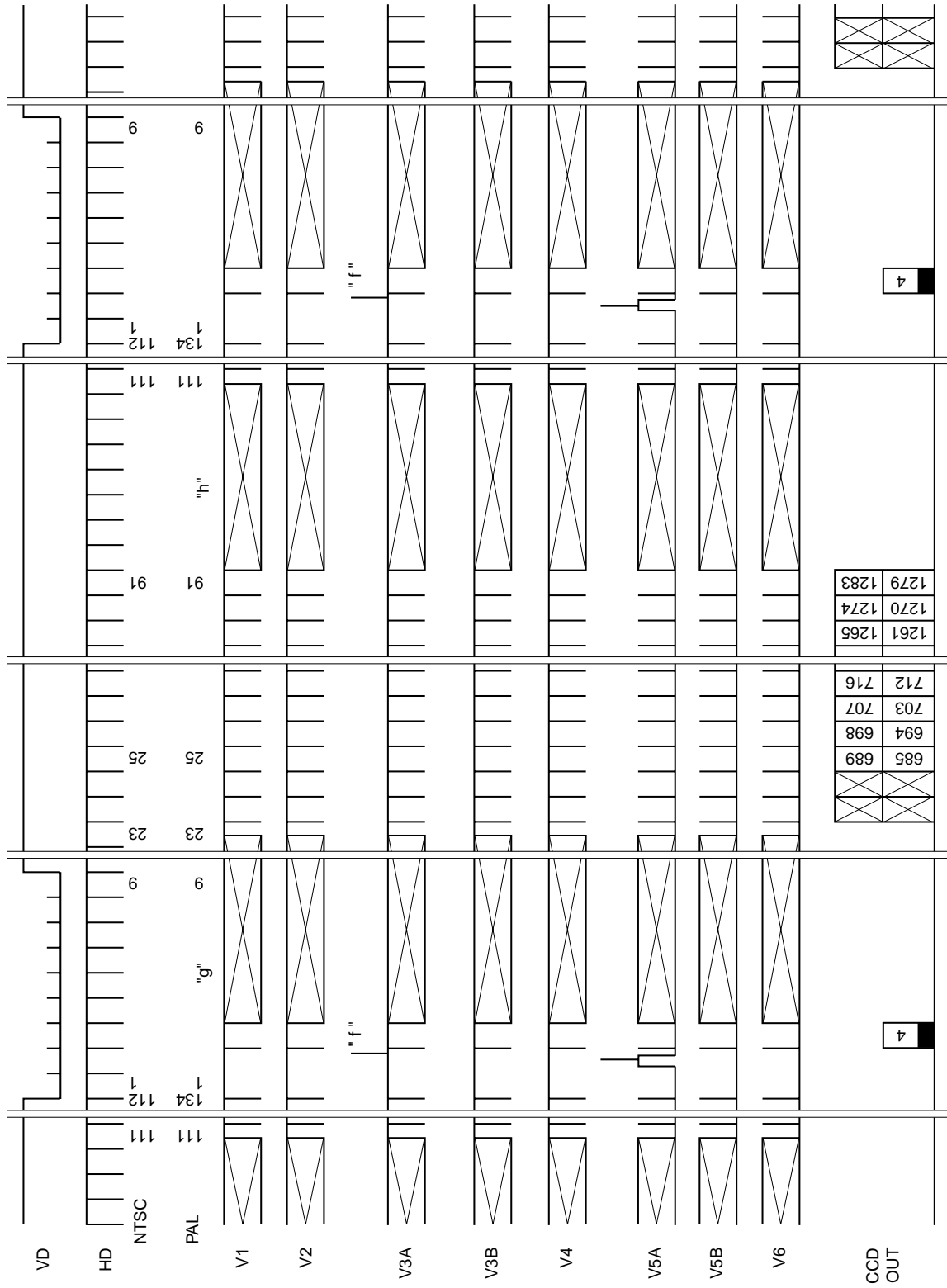


Drive Timing Chart (Vertical Sync) NTSC/PAL AF Mode (Upper)

(Vertical Sync "i" Enlarged)



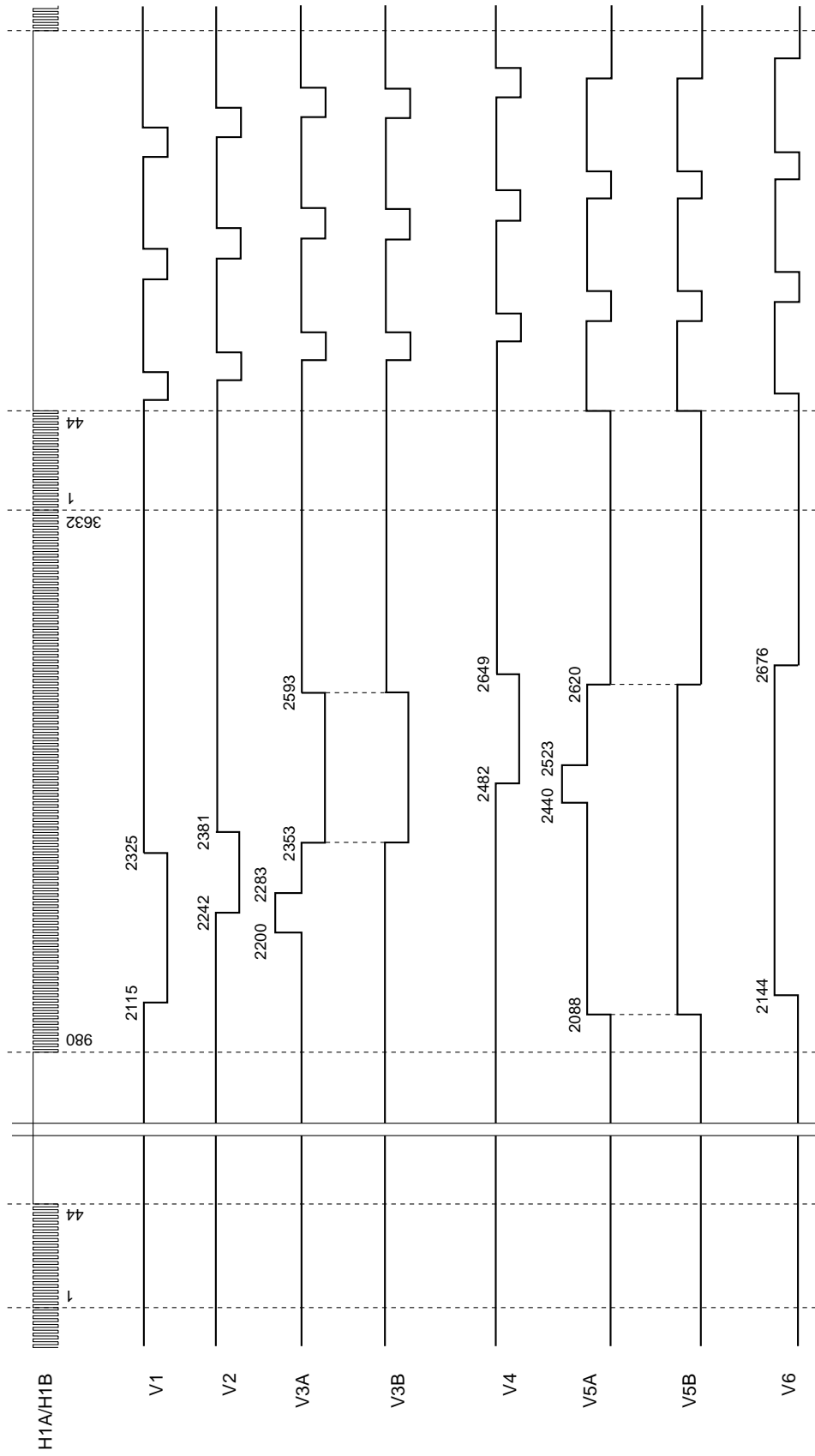
Drive Timing Chart (Vertical Sync) NTSC/PAL AF Mode (Center)



\* 3632fH, however, 112H in NTSC mode is 2253clk; 134H in PAL mode is 2944clk.

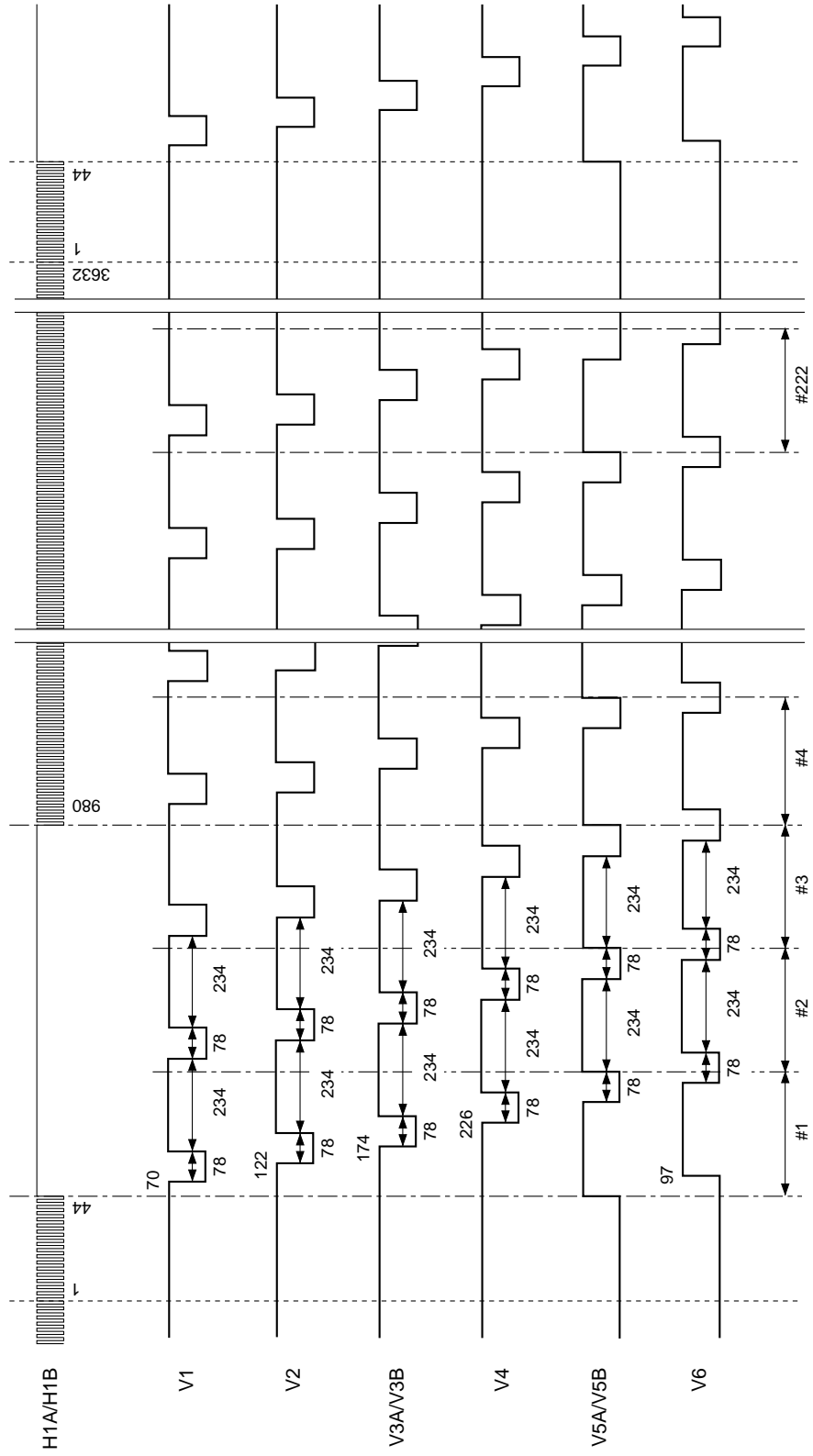
Drive Timing Chart (Vertical Sync) NTSC/PAL AF Mode (Center)

(Vertical Sync "f" Enlarged)



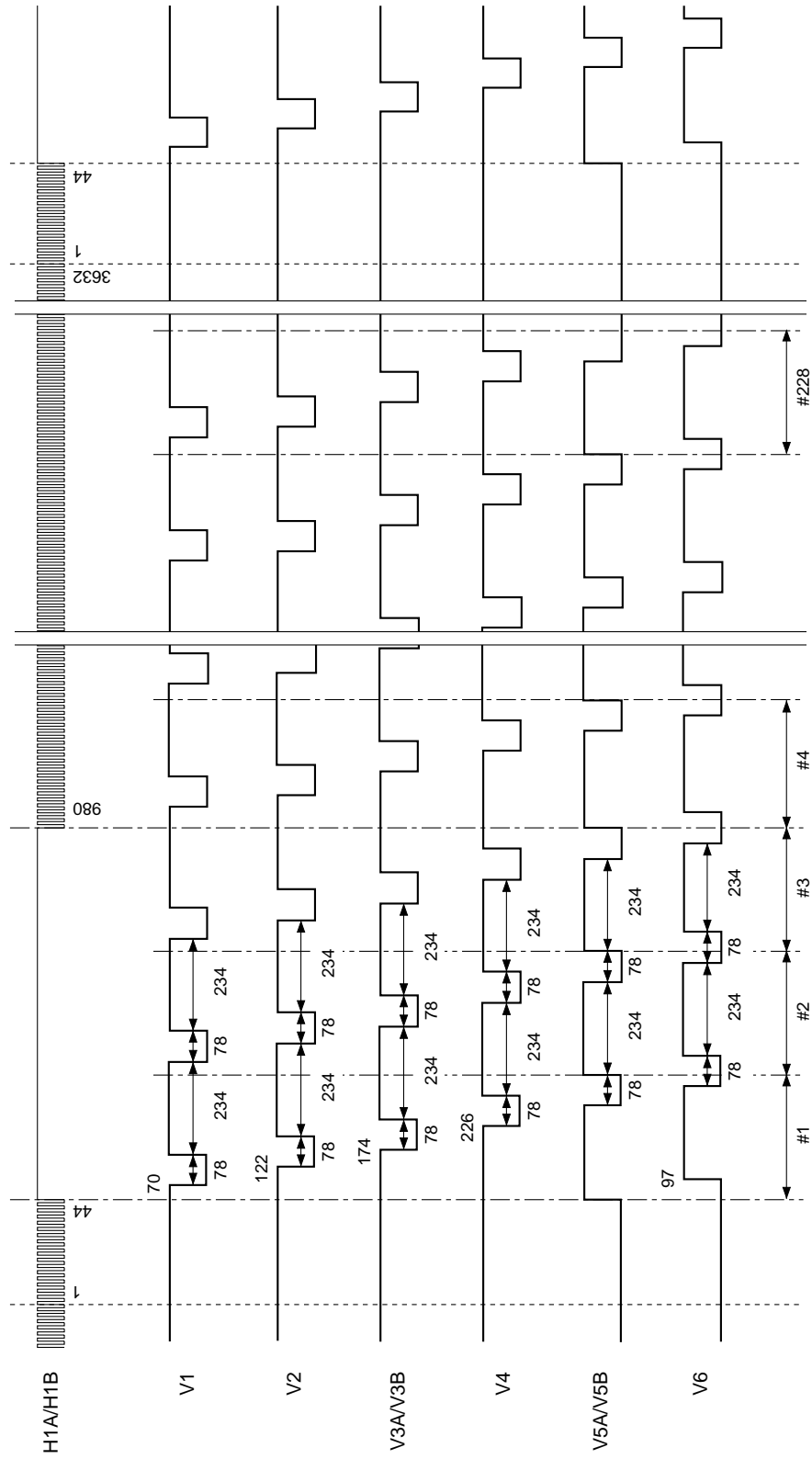
Drive Timing Chart (Vertical Sync) NTSC/PAL AF Mode (Center)

(Vertical Sync "g" Enlarged)



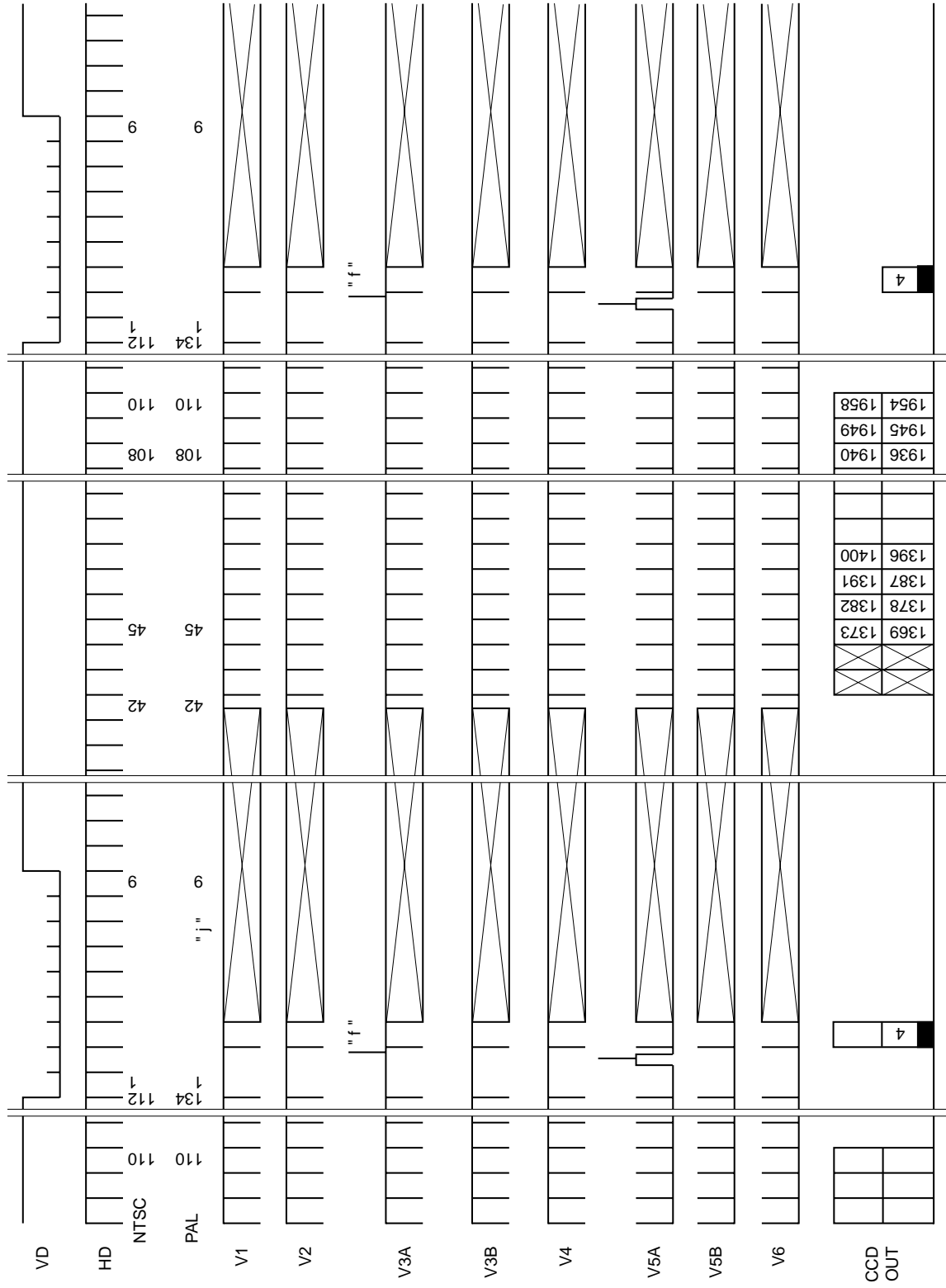
Drive Timing Chart (Vertical Sync) NTSC/PAL AF Mode (Center)

(Vertical Sync "h" Enlarged)





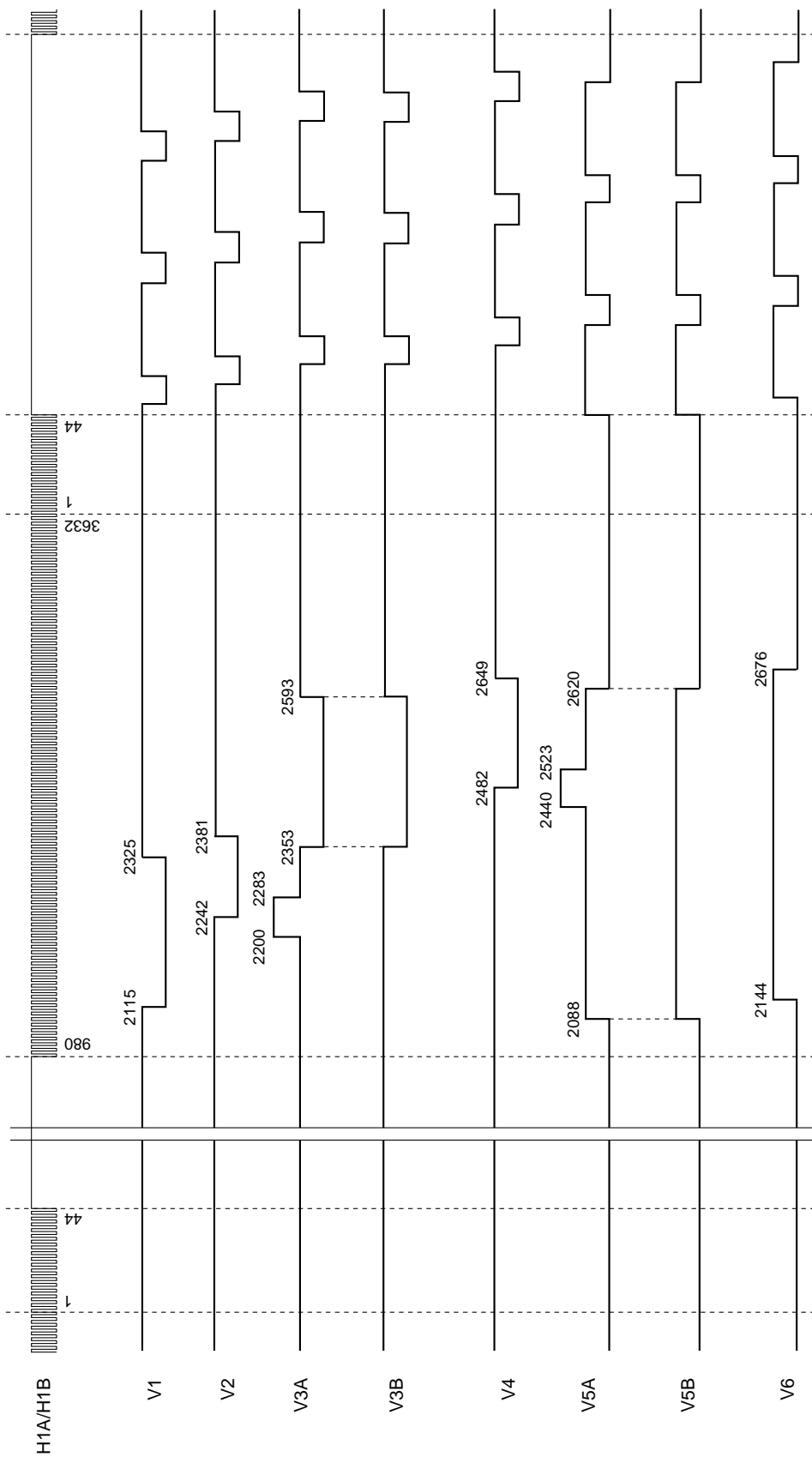
Drive Timing Chart (Vertical Sync) NTSC/PAL AF Mode (Lower)



\* 3632fH, however, 112H in NTSC mode is 2253clk; 134H in PAL mode is 2944clk.

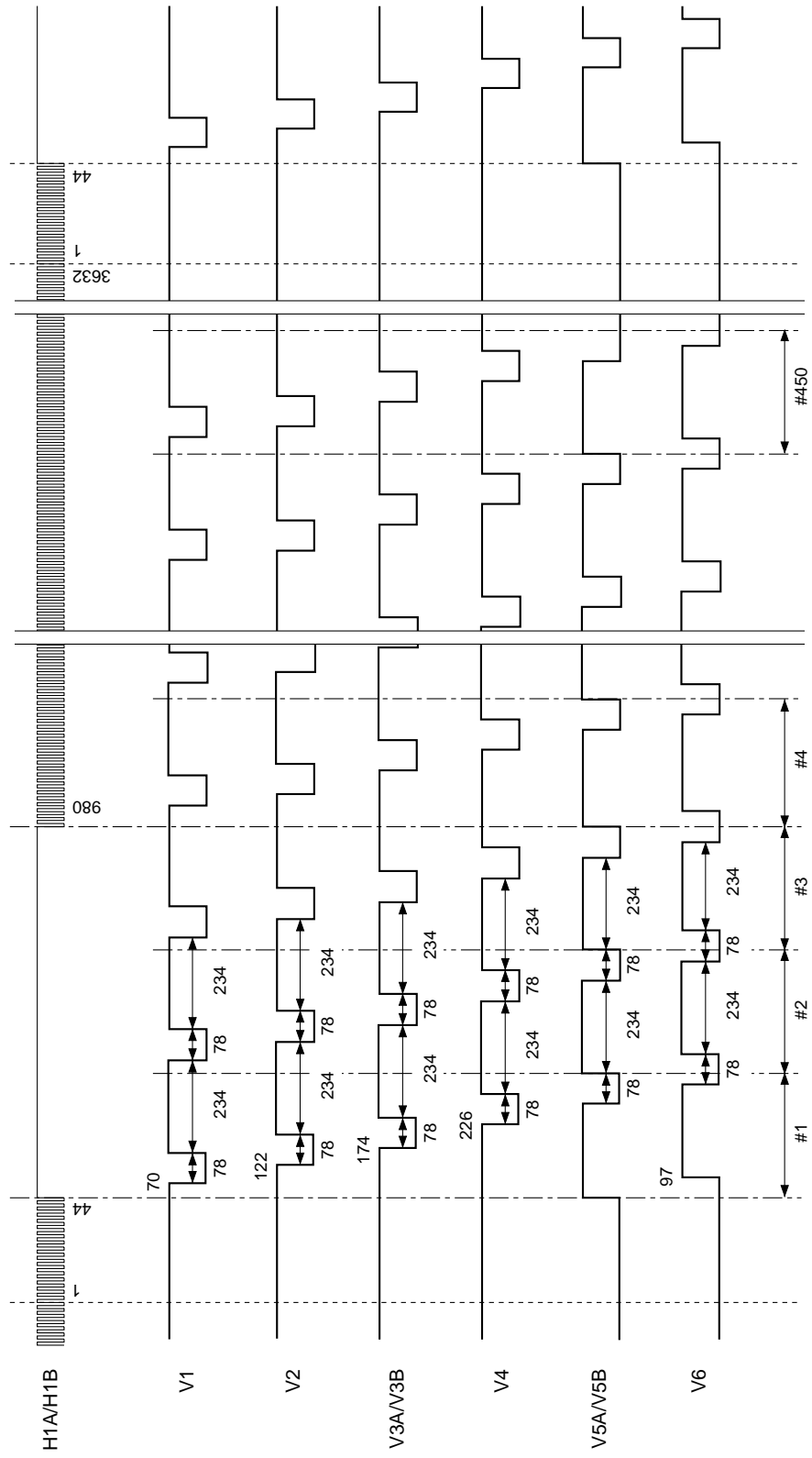
Drive Timing Chart (Vertical Sync) NTSC/PAL AF Mode (Lower)

(Vertical Sync "f" Enlarged)

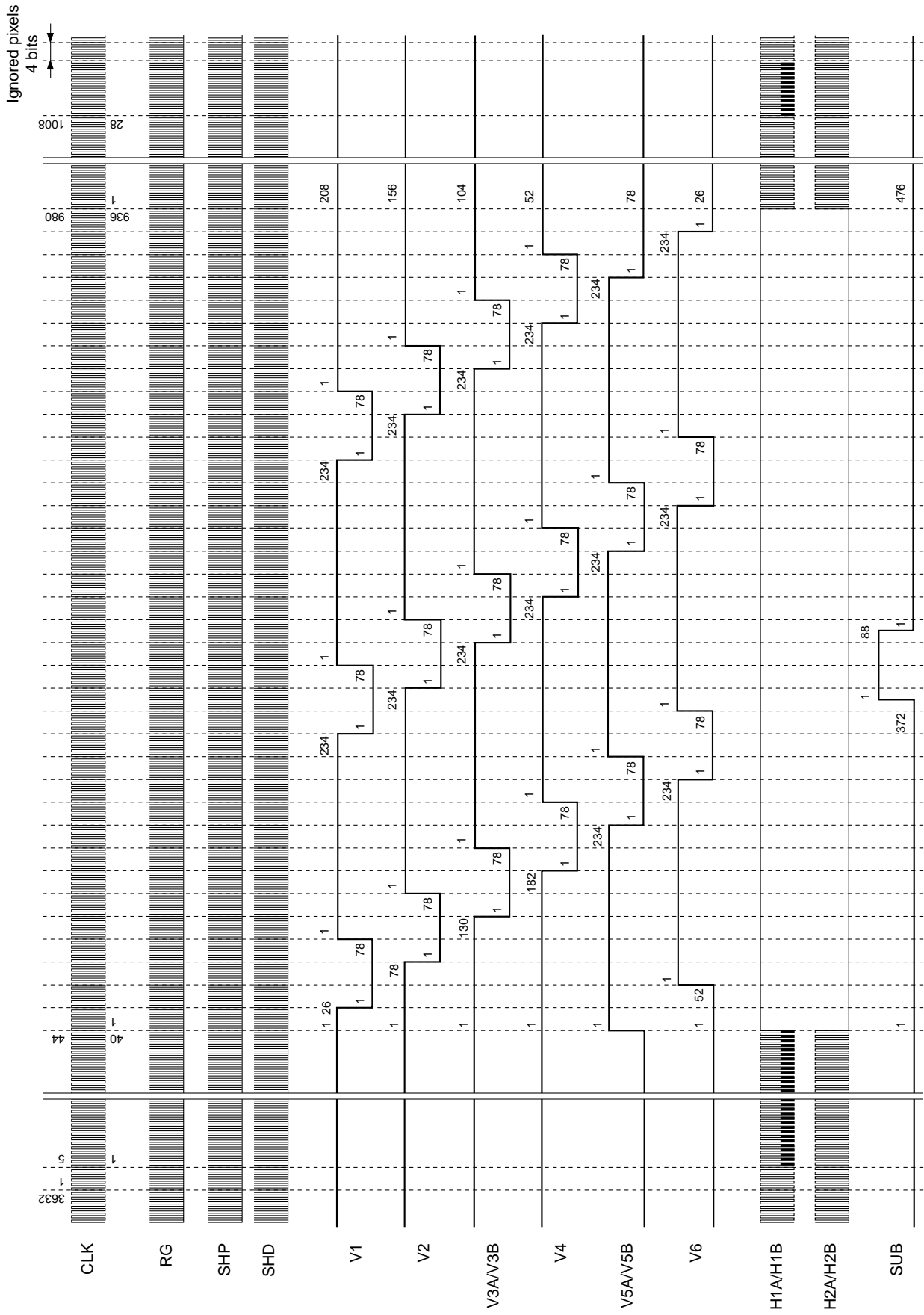


Drive Timing Chart (Vertical Sync) NTSC/PAL AF Mode (Lower)

(Vertical Sync "j" Enlarged)



Drive Timing Chart (Horizontal Sync) NTSC/PAL AF Mode



## Notes on Handling

### 1) Static charge prevention

CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

- a) Either handle bare handed or use non-chargeable gloves, clothes or material.  
Also use conductive shoes.
- b) When handling directly use an earth band.
- c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
- d) Ionized air is recommended for discharge when handling CCD image sensors.
- e) For the shipment of mounted substrates, use boxes treated for the prevention of static charges.

### 2) Soldering

- a) Make sure the package temperature does not exceed 80°C.
- b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a 30W soldering iron with a ground wire and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
- c) To dismount an image sensor, do not use a solder suction equipment. When using an electric desoldering tool, use a thermal controller of the zero-cross On/Off type and connect it to ground.

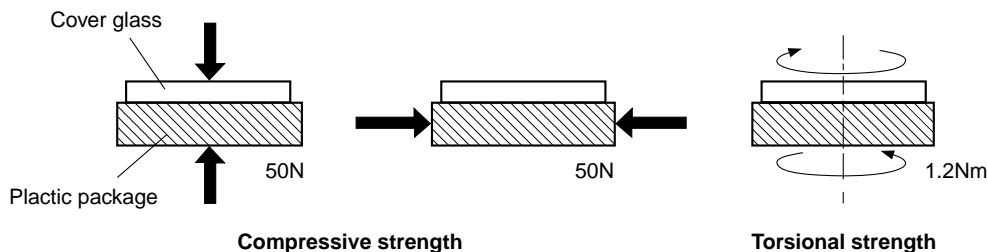
### 3) Dust and dirt protection

Image sensors are packed and delivered by taking care of protecting its glass plates from harmful dust and dirt. Clean glass plates with the following operations as required, and use them.

- a) Perform all assembly operations in a clean room (class 1000 or less).
- b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)
- c) Clean with a cotton bud and ethyl alcohol if grease stained. Be careful not to scratch the glass.
- d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
- e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

### 4) Installing (attaching)

- a) Remain within the following limits when applying a static load to the package. Do not apply any load more than 0.7mm inside the outer perimeter of the glass portion, and do not apply any load or impact to limited portions. (This may cause cracks in the package.)

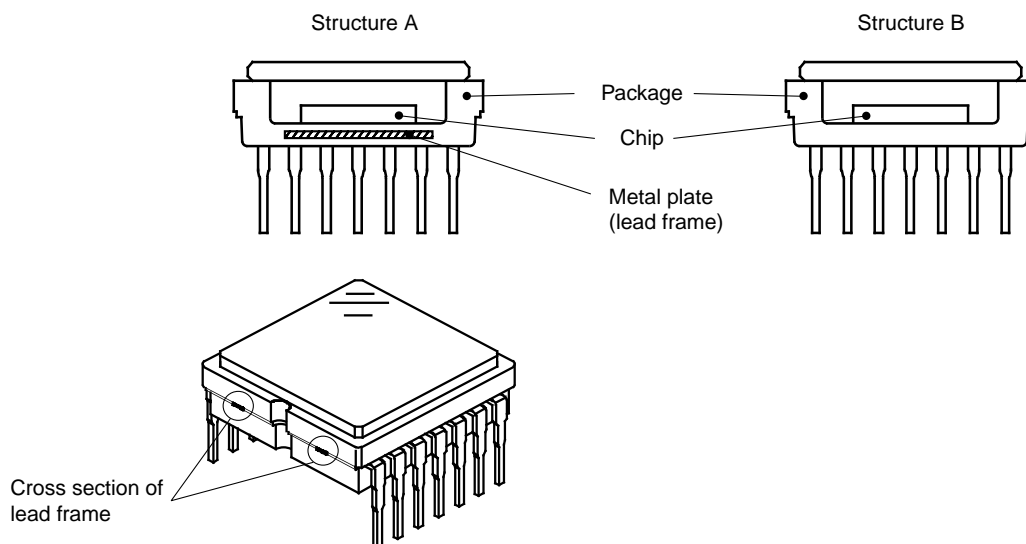


- b) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package. Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.

- c) The adhesive may cause the marking on the rear surface to disappear, especially in case the regulated voltage value is indicated on the rear surface. Therefore, the adhesive should not be applied to this area, and indicated values should be transferred to other locations as a precaution.
- d) The notch of the package is used for directional index, and that can not be used for reference of fixing. In addition, the cover glass and seal resin may overlap with the notch of the package.
- e) If the leads are bent repeatedly and metal, etc., clash or rub against the package, the dust may be generated by the fragments of resin.
- f) Acrylate anaerobic adhesives are generally used to attach CCD image sensors. In addition, cyanoacrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives. (reference)

#### 5) Others

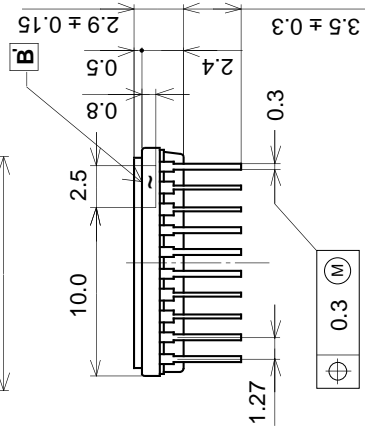
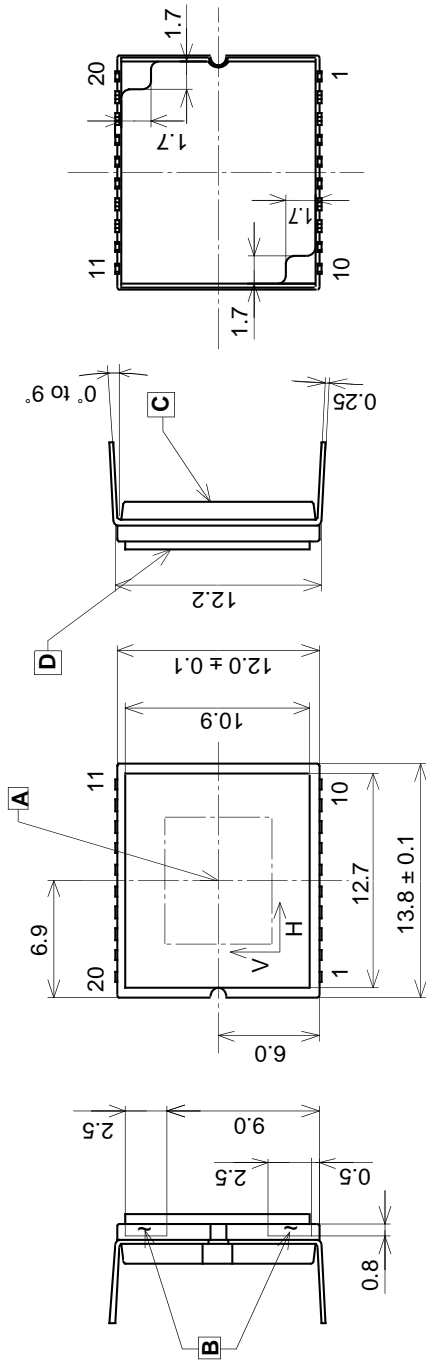
- a) Do not expose to strong light (sun rays) for long periods, as color filters will be discolored. When high luminous objects are imaged with the exposure level controlled by the electronic iris, the luminance of the image-plane may become excessive and discoloring of the color filter will possibly be accelerated. In such a case, it is advisable that taking-lens with the automatic-iris and closing of the shutter during the power-off mode should be properly arranged. For continuous using under cruel condition exceeding the normal using condition, consult our company.
- b) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.
- c) Brown stains may be seen on the bottom or side of the package. But this does not affect the CCD characteristics.
- d) This package has 2 kinds of internal structure. However, their package outline, optical size, and strength are the same.



The cross section of lead frame can be seen on the side of the package for structure A.

Package Outline Unit: mm

20 pin DIP



1. "A" is the center of the effective image area.
2. The two points "B" of the package are the horizontal reference. The point "B" of the package is the vertical reference.
3. The bottom "C" of the package, and the top of the cover glass "D" are the height reference.
4. The center of the effective image area relative to "B" and "B" is (H, V) = (6.9, 6.0) ± 0.075mm.
5. The rotation angle of the effective image area relative to H and V is ± 1°.
6. The height from the bottom "C" to the effective image area is 1.41 ± 0.10mm. The height from the top of the cover glass "D" to the effective image area is 1.49 ± 0.15mm.
7. The tilt of the effective image area relative to the bottom "C" is less than 50µm. The tilt of the effective image area relative to the top "D" of the cover glass is less than 50µm.
8. The thickness of the cover glass is 0.5mm, and the refractive index is 1.5.
9. The notches on the bottom of the package are used only for directional index, they must not be used for reference of fixing.

PACKAGE STRUCTURE

PACKAGE MATERIAL	Plastic
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	0.95g
DRAWING NUMBER	AS-B6-02(E)