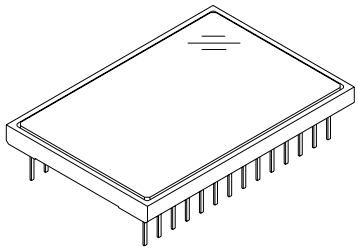
SONY

ICX263AL

Diagonal 28.42mm (Type 1.8) Frame Readout CCD Image Sensor with Square Pixel *Preliminary*

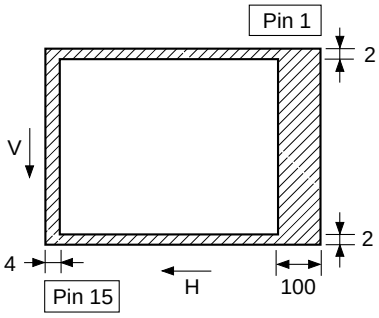
28 pin DIP (Ceramic)



Description

The ICX263AL is a diagonal 28.42mm (Type 1.8) image size interline CCD solid-state image sensor with a square pixel array and 10.66M effective pixels. This chip can support an output data rate up to 20MHz (max.) and a frame rate of approximately 1.6 frames/second.

This chip uses the frame readout method and features an electronic shutter with variable charge-storage time. In addition, high frame rate readout mode is also supported. Further, high sensitivity and low dark current are achieved through the adoption of HAD (Hole Accumulation Diode) sensors.



Optical black position (Top View)

Features

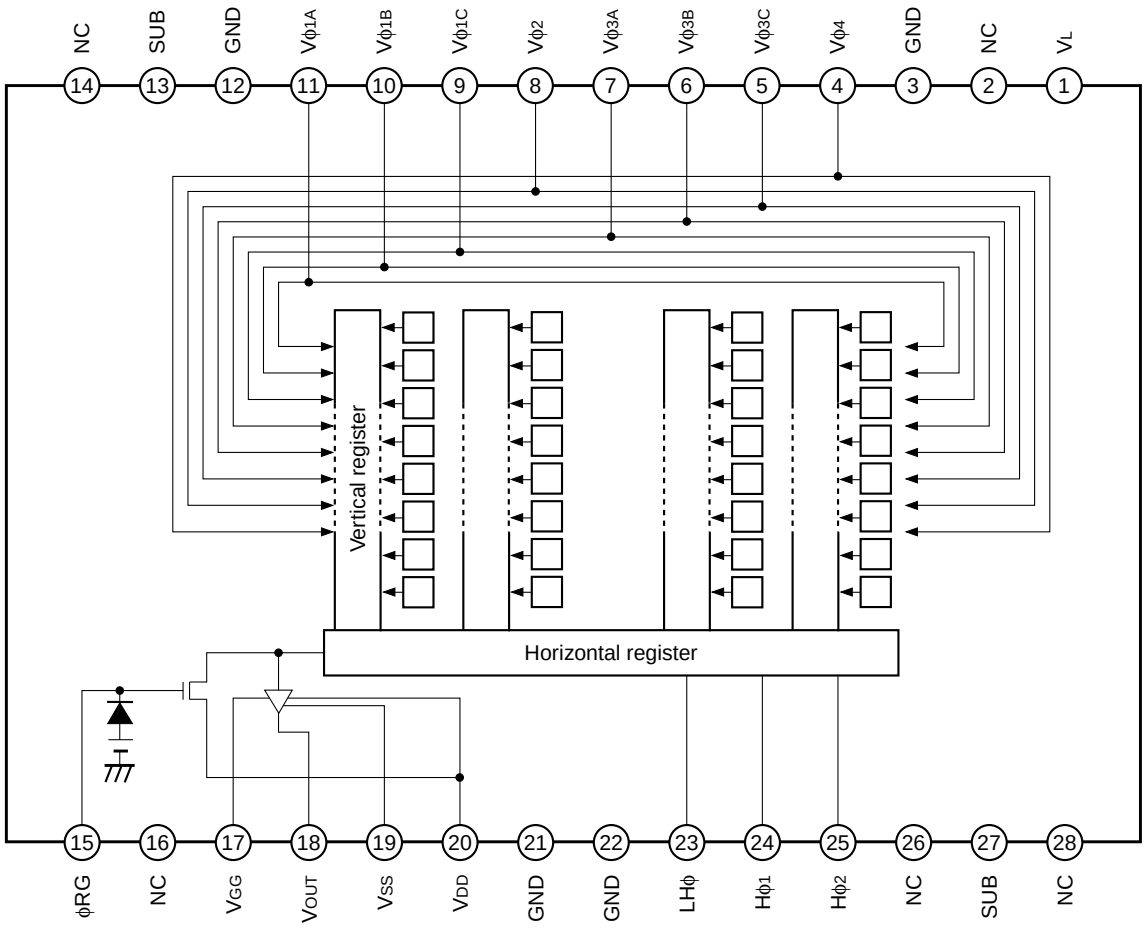
- Frame readout method
- High horizontal and vertical resolution
- Square pixel
- Maximum output data rate: 20MHz (frame rate: approximately 1.6)
- Maximum horizontal drive frequency: 20MHz
- Supports high frame rate readout mode (effective 441 lines output)
- Reset gate voltage not adjusted
- High sensitivity, low dark current
- Continuous variable-speed electronic shutter

Device Structure

- Interline CCD image sensor
- Image size: Diagonal 28.42mm (Type 1.8)
- Total number of pixels: 4128 (H) × 2652 (V) approx. 10.95M pixels
- Number of effective pixels: 4024 (H) × 2648 (V) approx. 10.66M pixels
- Number of active pixels: 4000 (H) × 2624 (V) approx. 10.50M pixels
- Chip size: 25.20mm (H) × 17.96mm (V)
- Unit cell size: 5.9µm (H) × 5.9µm (V)
- Optical black: Horizontal (H) direction: Front 4 pixels, rear 100 pixels
  Vertical (V) direction: Front 2 pixels, rear 2 pixels
- Number of dummy bits: Horizontal 20
  Vertical 1
- Substrate material: Silicon

PE01207-PS

Block Diagram and Pin Configuration (Top View)



Pin Description

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	V_L	Protective transistor bias	15	φRG	Reset gate clock
2	NC		16	NC	
3	GND	GND	17	V_{GG}	Output amplifier gate
4	Vφ4	Vertical register transfer clock	18	V_{OUT}	Signal output
5	Vφ3C	Vertical register transfer clock	19	V_{SS}	Output amplifier source
6	Vφ3B	Vertical register transfer clock	20	V_{DD}	Supply voltage
7	Vφ3A	Vertical register transfer clock	21	GND	GND
8	Vφ2	Vertical register transfer clock	22	GND	GND
9	Vφ1C	Vertical register transfer clock	23	LHφ	Horizontal register final stage transfer clock
10	Vφ1B	Vertical register transfer clock	24	Hφ1	Horizontal register transfer clock
11	Vφ1A	Vertical register transfer clock	25	Hφ2	Horizontal register transfer clock
12	GND	GND	26	NC	
13	SUB	Substrate (overflow drain)	27	SUB	Substrate (overflow drain)
14	NC		28	NC	

Absolute Maximum Ratings

Item		Rating	Unit	Remarks
Against SUB	V_{DD}, V_{OUT}, φRG – SUB	–40 to +10	V	
	$V\phi_{1A}$, $V\phi_{1B}$, $V\phi_{1C}$, $V\phi_{3A}$, $V\phi_{3B}$, $V\phi_{3C}$ – SUB	–50 to +15	V	
	$V\phi_2$, $V\phi_4$, V_L – SUB	–50 to +0.3	V	
	$H\phi_1$, $H\phi_2$, LHφ, GND – SUB	–40 to +0.3	V	
Against GND	V_{DD}, V_{OUT}, φRG – GND	–0.3 to +18	V	
	$V\phi_{1A}$, $V\phi_{1B}$, $V\phi_{1C}$, $V\phi_{3A}$, $V\phi_{3B}$, $V\phi_{3C}$ – GND	–10 to +18	V	
	$V\phi_2$, $V\phi_4$, V_L – GND	–10 to +18	V	
	$H\phi_1$, $H\phi_2$, LHφ – GND	–10 to +7	V	
Against V_L	$V\phi_{1A}$, $V\phi_{1B}$, $V\phi_{1C}$, $V\phi_{3A}$, $V\phi_{3B}$, $V\phi_{3C}$ – V_L	–0.3 to +28	V	
	$V\phi_2$, $V\phi_4$, $H\phi_1$, $H\phi_2$, LHφ, GND – V_L	–0.3 to +17	V	
Between input clock pins	Voltage difference between vertical clock input pins	to +15	V	*1
	$H\phi_1$ – $H\phi_2$	–7 to +7	V	
	$H\phi_1$, $H\phi_2$ – $V\phi_4$	–17 to +17	V	
Storage temperature		–30 to +80	°C	
Guaranteed temperature of performance		–10 to +60	°C	
Operating temperature		–10 to +75	°C	

*1 +27V (Max.) is guaranteed when clock width < 10µs, clock duty factor < 0.1%.

Bias Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage	V_{DD}	14.55	15.0	15.45	V	
Output amplifier gate voltage	V_{GG}	5.5	6.0	6.5	V	
Output amplifier source	V_{SS}	Connected to GND via resistance of 200 to 600Ω				
Substrate voltage adjustment range	V_{SUB}	8.5		15.0	V	
Protective transistor bias	V_L	*2				
Reset gate clock	φRG	*3				

*2 V_L setting is the V_{VL} voltage of the vertical clock waveform, or the same voltage as the V_L power supply for the V driver should be used.

*3 Do not apply a DC bias to the reset gate clock pin, because a DC bias is generated within the CCD.

DC characteristics

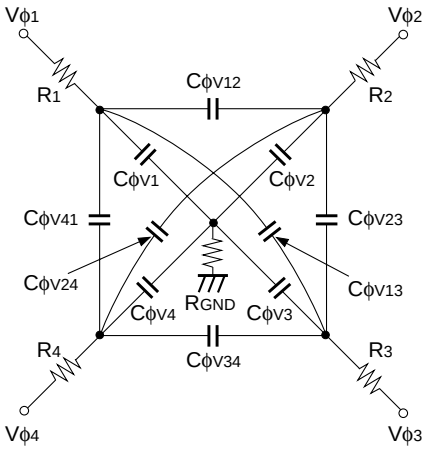
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply current	I_{DD}		8.7		mA	

Clock Voltage Conditions

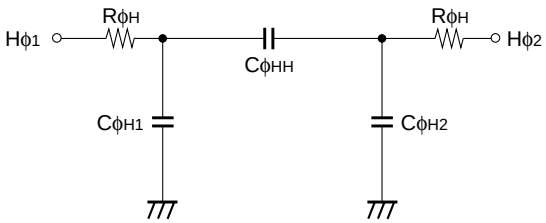
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Readout clock voltage	V_{VT}	14.55	15.0	15.45	V	
Vertical transfer clock voltage	V_{VH}	–0.05	0	0.05	V	
	V_{VL}	–9.5	–9.0	–8.5	V	
Horizontal transfer clock voltage	$V\phi_H$	6.0			V	Absolute maximum voltage value ≤ 8.0V
	V_{HL}	–0.25	0	0.25	V	
Horizontal final stage transfer clock voltage	V_{LHH}	7.6	8.0	8.4	V	
	V_{LHL}	–2.25	–2.0	–1.75	V	
Reset gate clock voltage	$V\phi_{RG}$	4.5	5.0	5.5	V	
Substrate clock voltage	$V\phi_{SUB}$	23.05	24.0	24.95	V	

Clock Equivalent Circuit Constants

Item	Symbol	Typ.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C\phi_{V1}$, $C\phi_{V3}$	21000	pF	
	$C\phi_{V2}$, $C\phi_{V4}$	12000	pF	
Capacitance between vertical transfer clocks	$C\phi_{V12}$, $C\phi_{V34}$	8500	pF	
	$C\phi_{V23}$, $C\phi_{V41}$	7100	pF	
	$C\phi_{V13}$	3100	pF	
	$C\phi_{V24}$	1700	pF	
Capacitance between horizontal transfer clock and GND	$C\phi_{H1}$	230	pF	
	$C\phi_{H2}$	180	pF	
Capacitance between horizontal transfer clocks	$C\phi_{HH}$	300	pF	
Capacitance between horizontal final stage transfer clock and GND	$C\phi_{LH}$	8	pF	
Capacitance between reset gate clock and GND	$C\phi_{RG}$	6	pF	
Capacitance between substrate clock and GND	$C\phi_{SUB}$	4700	pF	
Vertical transfer clock series resistor	R_1, R_2, R_3, R_4	20	Ω	
Vertical transfer clock ground resistor	R_{GND}	30	Ω	
Horizontal transfer clock series resistor	$R\phi_H$	0.6	Ω	



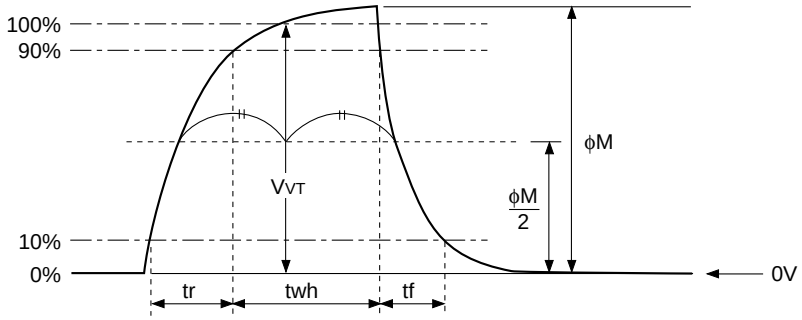
Vertical transfer clock equivalent circuit



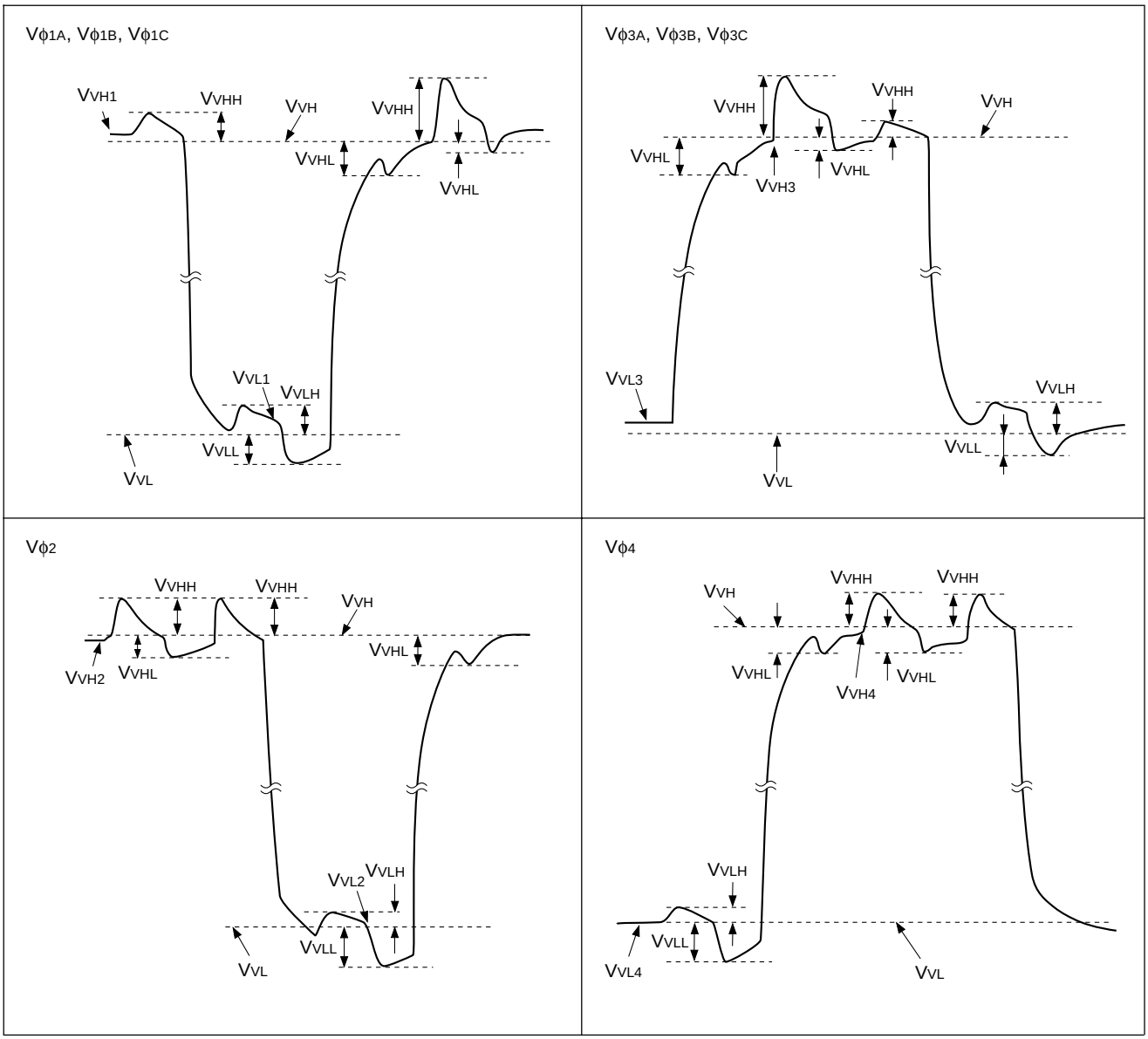
Horizontal transfer clock equivalent circuit

Drive Clock Waveform Conditions

(1) Readout clock waveform



(2) Vertical transfer clock waveform

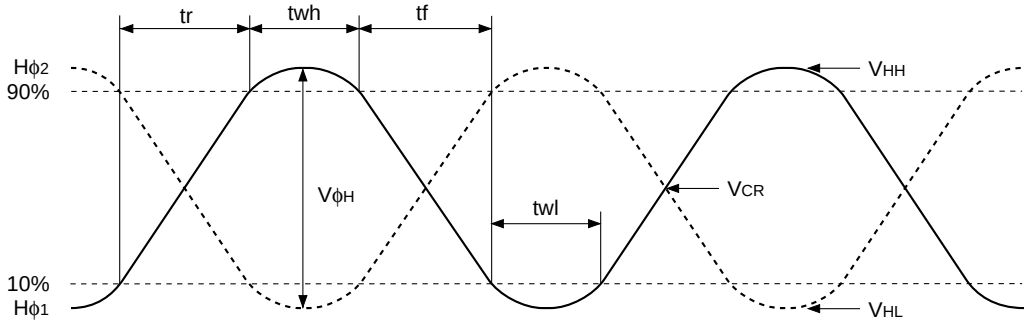


$V_{VH} = (V_{VH1} + V_{VH2})/2$

$V_{VL} = (V_{VL3} + V_{VL4})/2$

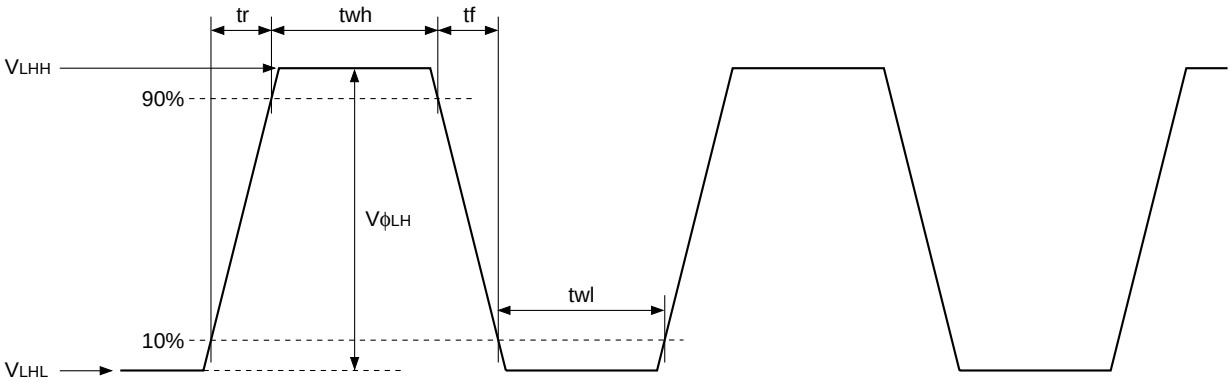
$V_{\phi V} = V_{VHn} – V_{VHn}$ (n = 1 to 4)

(3) Horizontal transfer clock waveform

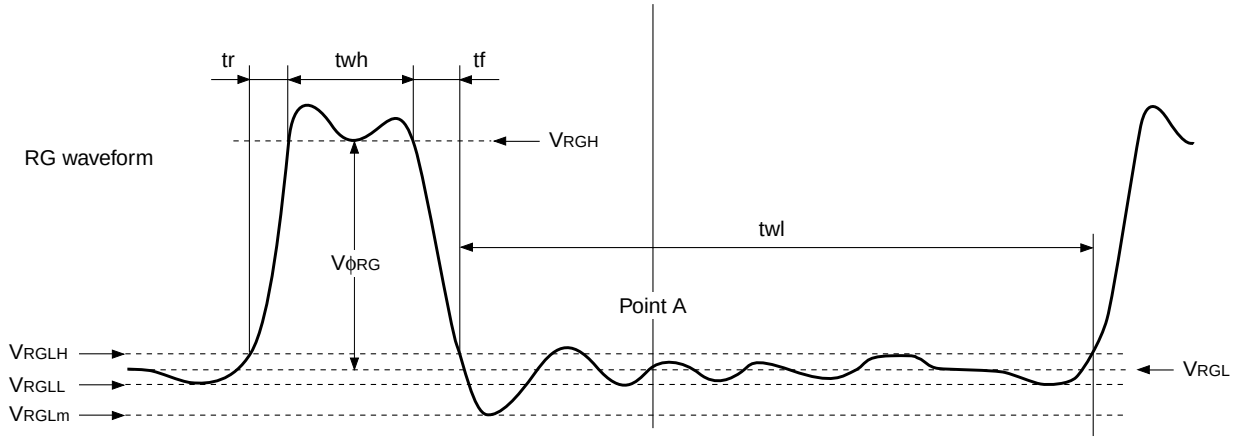


Cross-point voltage for the Hϕ1 rising side of the horizontal transfer clocks Hϕ1 and Hϕ2 waveforms is VCR.

(4) Horizontal final stage transfer clock waveform



(5) Reset gate clock waveform



VRGLH is the maximum value and VRGLL is the minimum value of the coupling waveform during the period from Point A in the above diagram until the rising edge of RG.

In addition, VRGL is the average value of VRGLH and VRGLL.

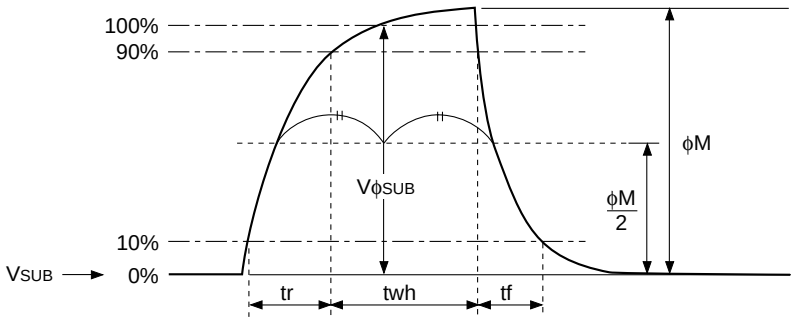
$$V_{RGL} = (V_{RGLH} + V_{RGLL})/2$$

Assuming VRGH is the minimum value during the interval twh, then:

$$V_{\phi RG} = V_{RGH} - V_{RGL}$$

Negative overshoot level during the falling edge of RG is VRGLm.

(6) Substrate clock waveform



Clock Switching Characteristics

Item	Symbol	twh			twl			tr			tf			Unit	Remarks
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Readout clock	V_T		5.5						1.5			1.5		µs	During readout
Vertical transfer clock	$V\phi_{1A}$, $V\phi_{1B}$, $V\phi_{1C}$, $V\phi_2$, $V\phi_{3A}$, $V\phi_{3B}$, $V\phi_{3C}$, $V\phi_4$								2			2		µs	When using CXD1268M
Horizontal transfer clock	$H\phi_1$, $H\phi_2$		17			17			8			8		ns	
Horizontal final stage transfer clock	$LH\phi$		22			22			3			3		ns	*1
Reset gate clock	ϕRG		7						2.5			2.5		ns	
Substrate clock	ϕSUB		3.0											µs	During drain charge

*1 Be sure to match the phases of the amplitude level 50% of the horizontal final stage transfer clock and the amplitude level 50% of horizontal transfer clock $H\phi_2$.

Image Sensor Characteristics (Ta = 25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks
Sensitivity	S	320	400		mV	1	1/60s accumulation, F5.6
Saturation signal	Vsat	500			mV	2	Ta = 60°C
Smear	Sm		0.001	0.003	%	3	No electronic shutter
Video signal shading*1	Sh			20	%	4	Zone I
				25	%	4	Zone II
Dark signal	Vdt			17	mV	5	Ta = 60°C, 1.6 frame/s
Dark signal shading	ΔVdt			28	mV	6	Ta = 60°C, 1.6 frame/s
Lag	Lag			0.5	%	7	
Maximum frame rate				1.6	/s		Horizontal drive frequency: 20MHz

*1 Video signal shading is the value with parallel incident light and a lens aperture value of F5.6 to F8.

◎ **Zone Definition of Video Signal Shading**

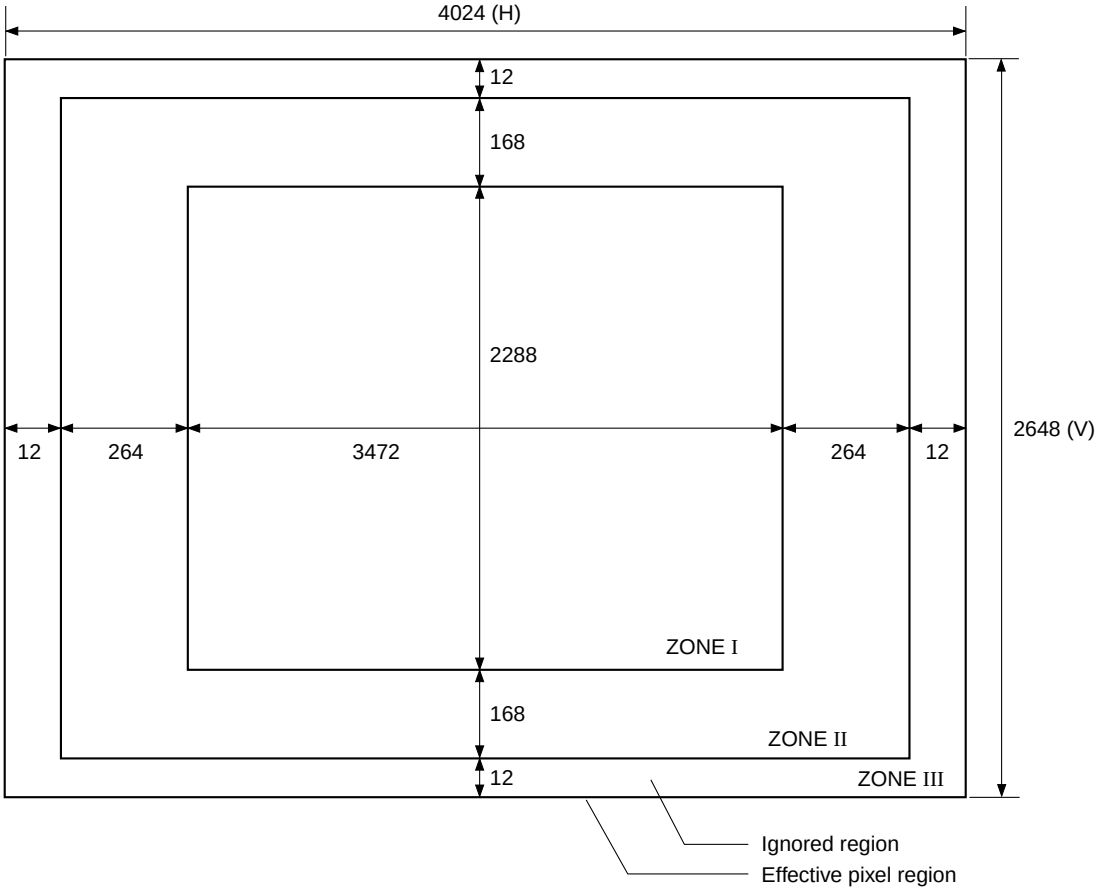


Image Sensor Characteristics Measurement Method

◎ **Measurement conditions**

(1) In the following measurements, the device drive conditions are at the typical values of the bias and clock voltage conditions, and the frame readout mode is used.

(2) In the following measurements, spot blemishes are excluded and, unless otherwise specified, the optical black level (OB) is used as the reference for the signal output, which is taken as the value measured at the output point (CCD OUT) shown in the drive circuit.

◎ **Definition of standard imaging conditions**

(1) Standard imaging condition I:
Use a pattern box (luminance: 706cd/m^2, color temperature of 3200K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter and image at F5.6. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

(2) Standard imaging condition II:
Image a light source (color temperature of 3200K) with a uniformity of brightness within 2% at all angles. Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

1. Sensitivity
Set to standard imaging condition I. After setting the electronic shutter mode with a shutter speed of 1/60s, measure the signal output at the center of the screen.

2. Saturation signal
Set to standard imaging condition II. After adjusting the luminous intensity to 20 times the intensity with the average value of the signal output, 150mV, measure the minimum value of the signal output.

3. Smear
Set to standard imaging condition II. With the lens diaphragm at F5.6 to F8, first adjust the luminous intensity to 500 times the intensity with the average value of signal output, 150mV. After the readout clock is stopped and the charge drain is executed by the electronic shutter at the respective H blankings, measure the maximum value (Vsm [mV]) of the signal output and substitute the value into the following formula.

$$Sm = \frac{Vsm}{150} \times \frac{1}{500} \times \frac{1}{10} \times 100 \text{ [\%]}$$ (1/10V method conversion value)

4. Video signal shading
   Set to standard imaging condition II. With the lens diaphragm at F5.6 to F8, input parallel light with an exit pupil distance of near infinity to the CCD image surface and adjust the luminous intensity so that the average value of the signal output is 150mV. Then measure the maximum value (Vmax [mV]) and minimum value (Vmin [mV]) of the signal output and substitute the values into the following formula.

   $Sh = (Vmax - Vmin)/150 \times 100$ [%]

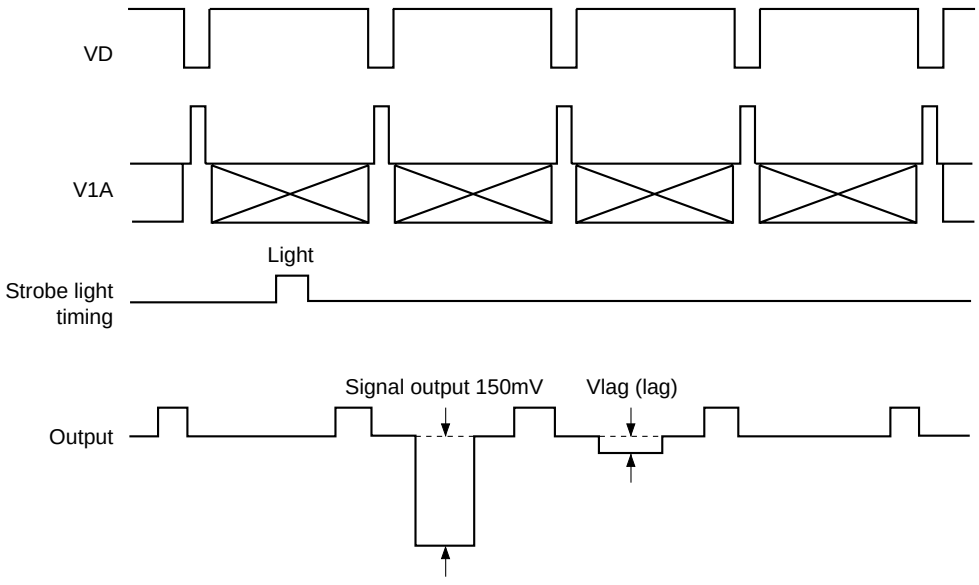
5. Dark signal
   Measure the average value of the signal output (Vdt [mV]) with the device ambient temperature 60°C and the device in the light-obstructed state, using the horizontal idle transfer level as a reference.

6. Dark signal shading
   After measuring 5, measure the maximum (Vdmax [mV]) and minimum (Vdmin [mV]) values of the dark signal output and substitute the values into the following formula.

   $\Delta Vdt = Vdmax - Vdmin$ [mV]

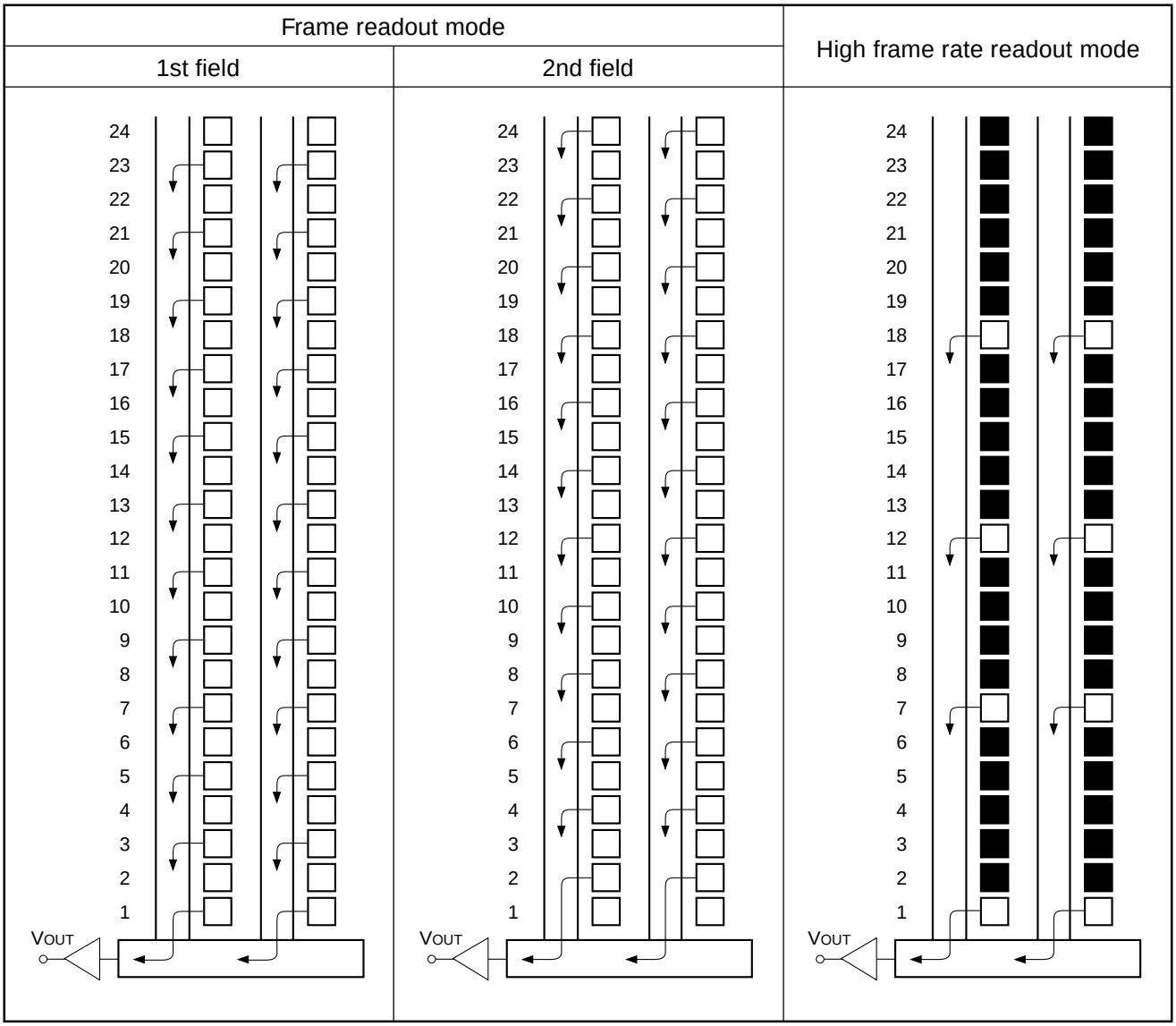
7. Lag
   Adjust the signal output generated by strobe light to 150mV. After setting the strobe light so that it strobes with the following timing, measure the residual signal (Vlag). Substitute the value into the following formula.

   $Lag = (Vlag/150) \times 100$ [%]



◎ Readout modes

The output methods for the following two readout modes are shown below.

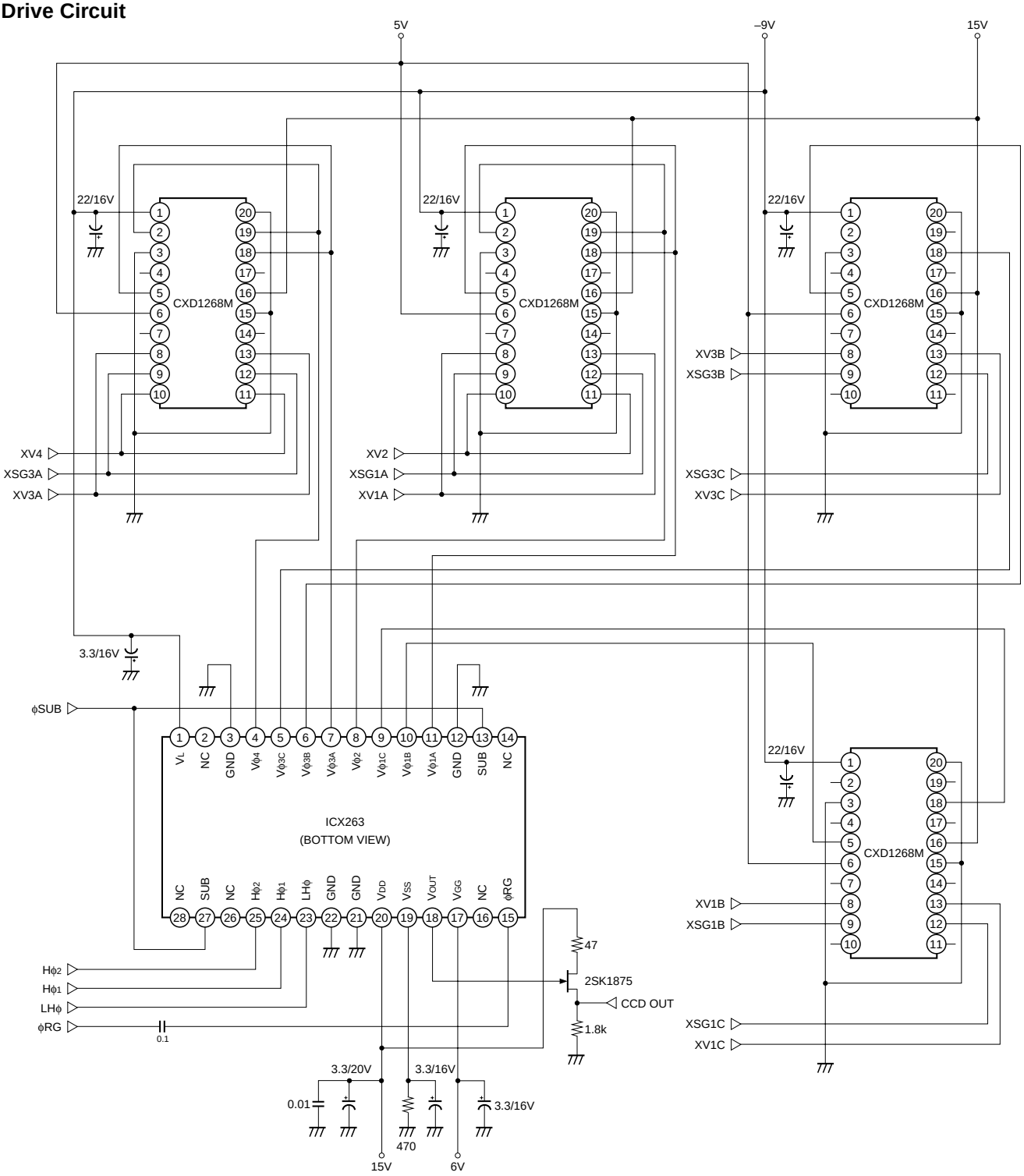


Note) Blacked out portions in the diagram indicate pixels which are not read out.
Output starts from line 1 in high frame rate readout mode.

1. Frame readout mode
   In this mode, all pixel signals are divided into two fields and output.
   All pixel signals are read out independently, making this mode suitable for high resolution image capturing.

2. High frame rate readout mode
   Output is performed at approximately 9 frames/s by reading out 4 out of 24 vertical pixels.
   The number of output lines is 441 lines.
   This readout mode emphasizes processing speed over vertical resolution.

Drive Circuit



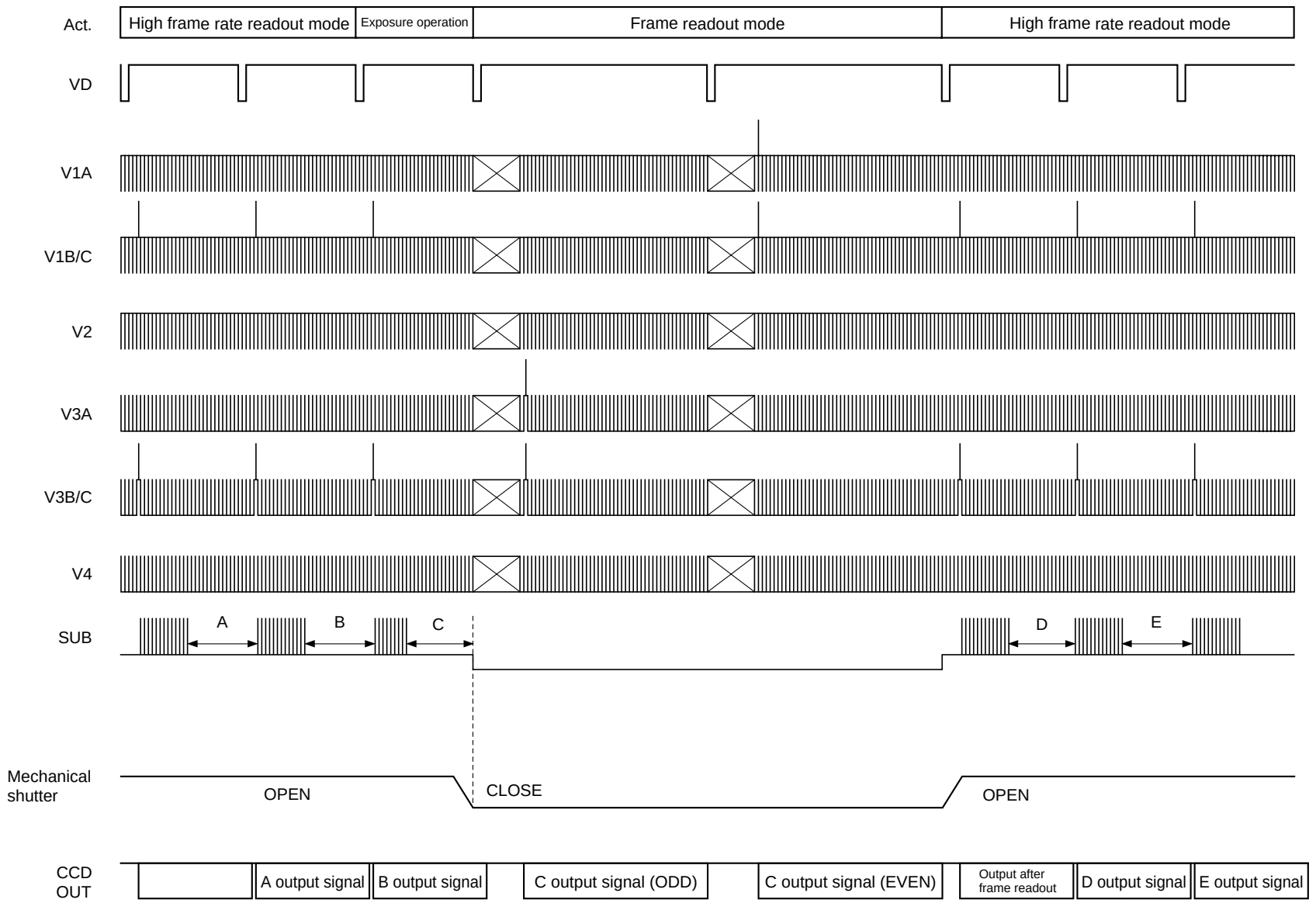
Notes) Substrate bias control

The saturation signal level decreases when exposure is performed using the mechanical shutter, so control the substrate bias.

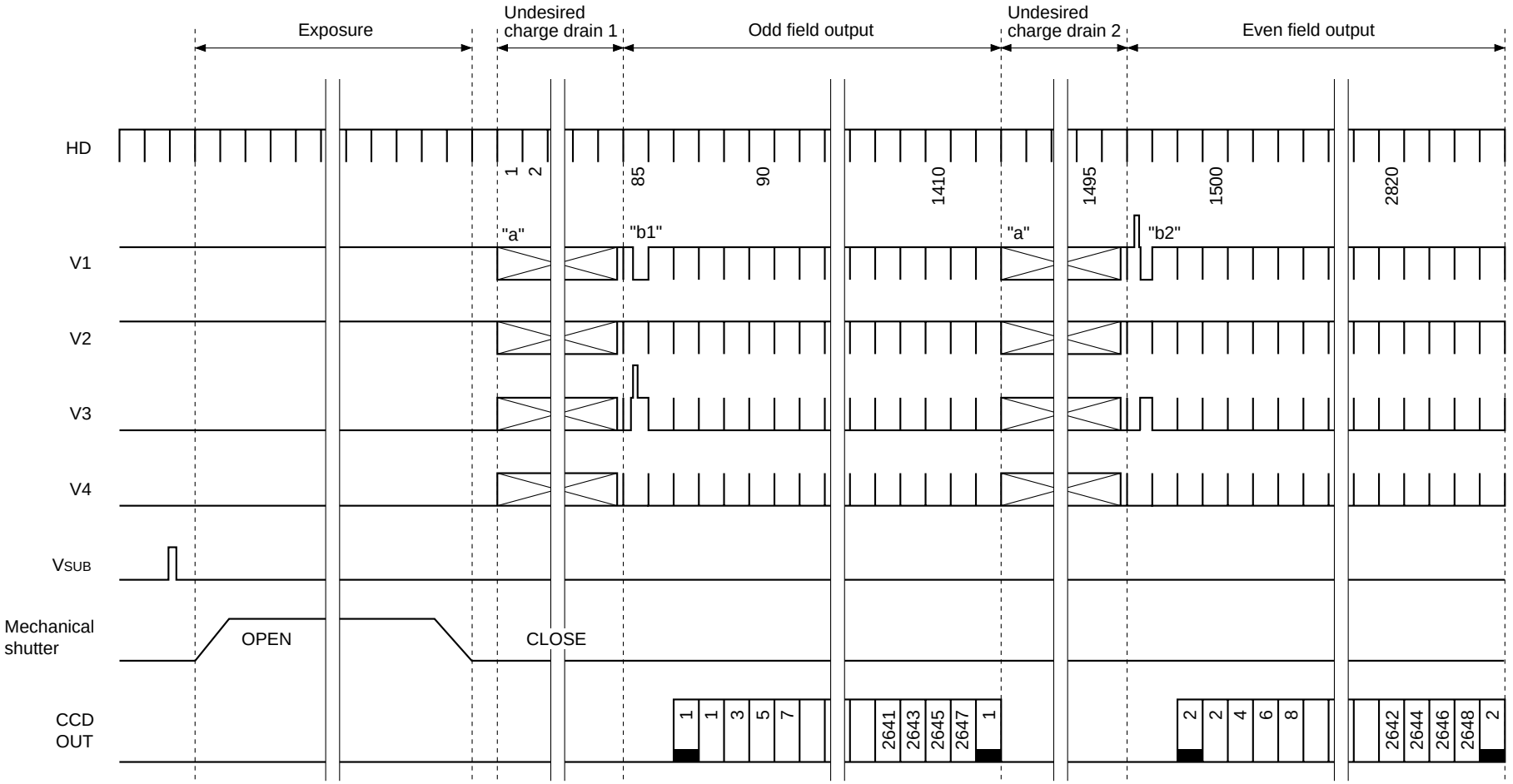
Drive timing precautions

The blooming signal generated during exposure in mechanical shutter mode is swept by providing two fields of idle transfer through vertical register high-speed sweep transfer from the time the mechanical shutter closes until sensor readout is performed. However, note that the V_L potential and the ϕSUB pin DC voltage sag at this time.

Drive Timing Chart (Vertical Sequence) High Frame Rate Readout Mode → Frame Readout Mode/Electronic Shutter Normal Operation

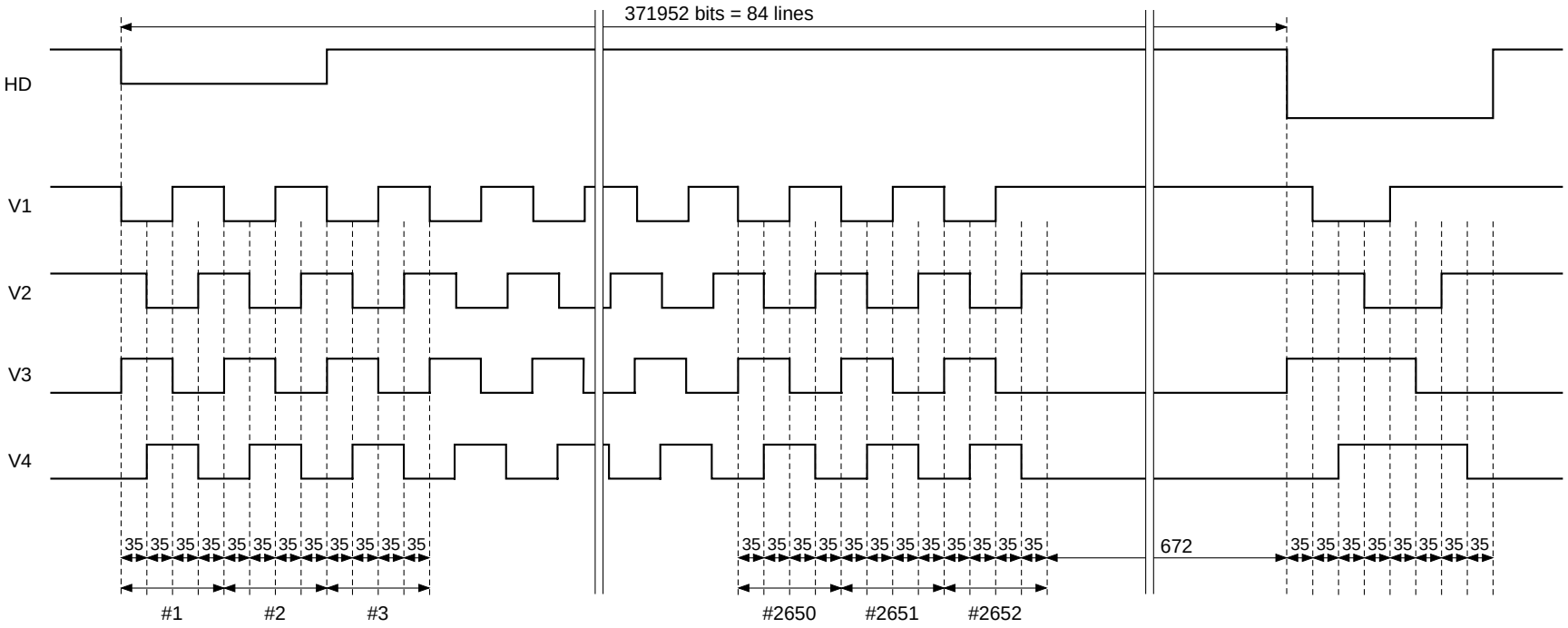


Drive Timing Chart (Vertical Sync) Frame Readout Mode



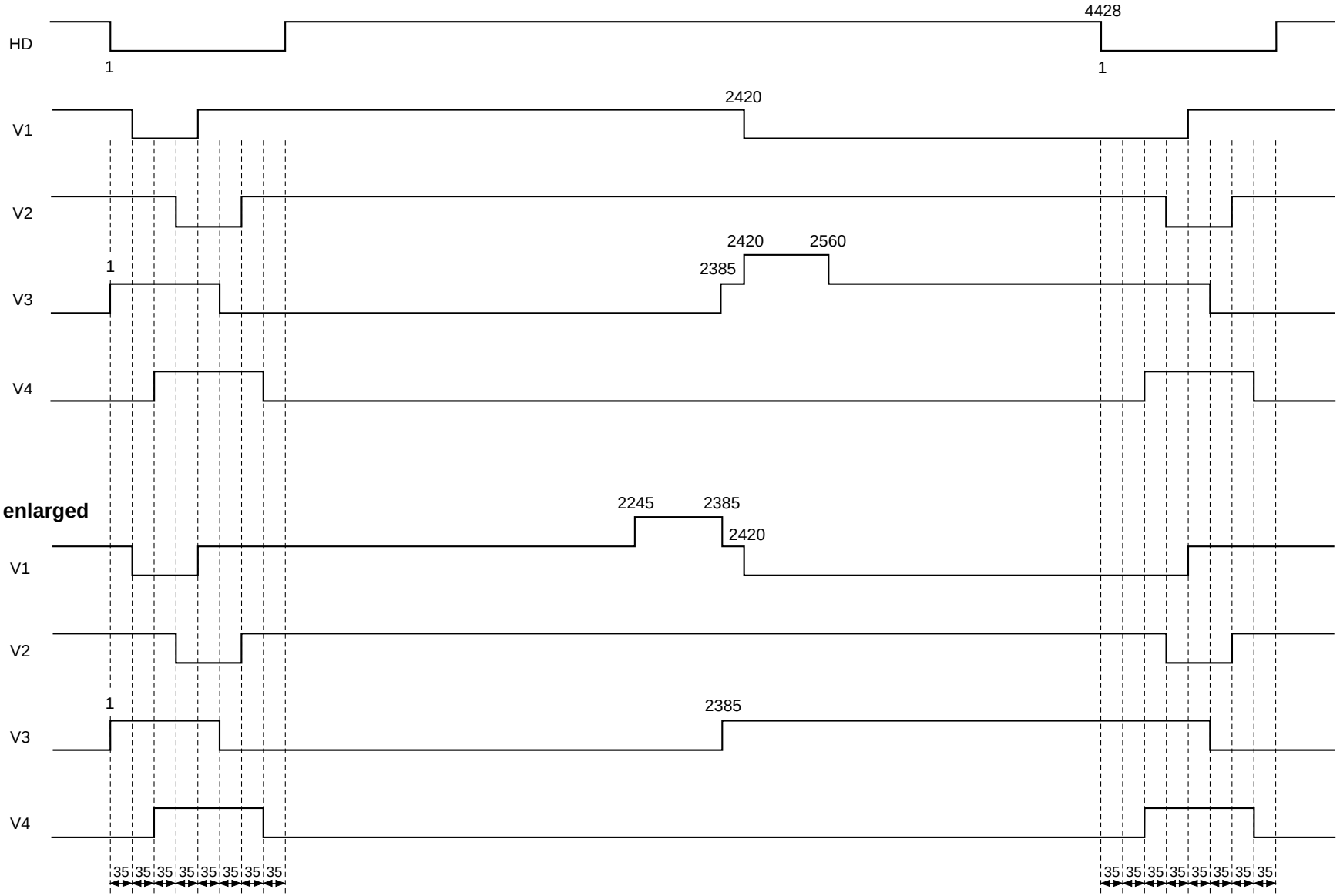
Note) Number of effective vertical pixels: 2648 (1 frame), number of vertical optical black pixels: front 2, rear 2 (1 frame)

Drive Timing Chart (Vertical Sync “a” Enlarged, Undesired Charge Drain)

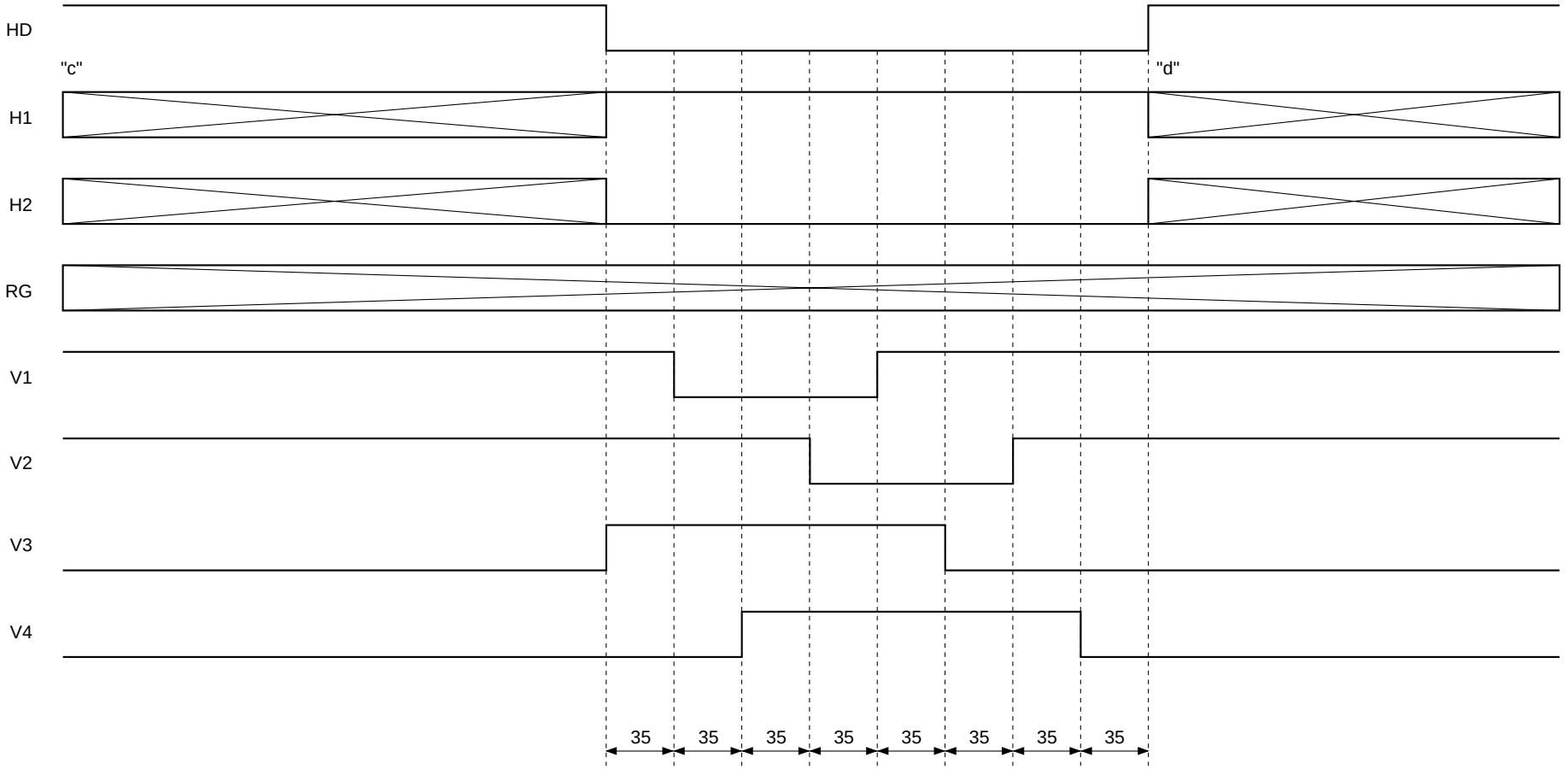


Drive Timing Chart (Vertical Sync “b1” and “b2” Enlarged, Sensor Readout)

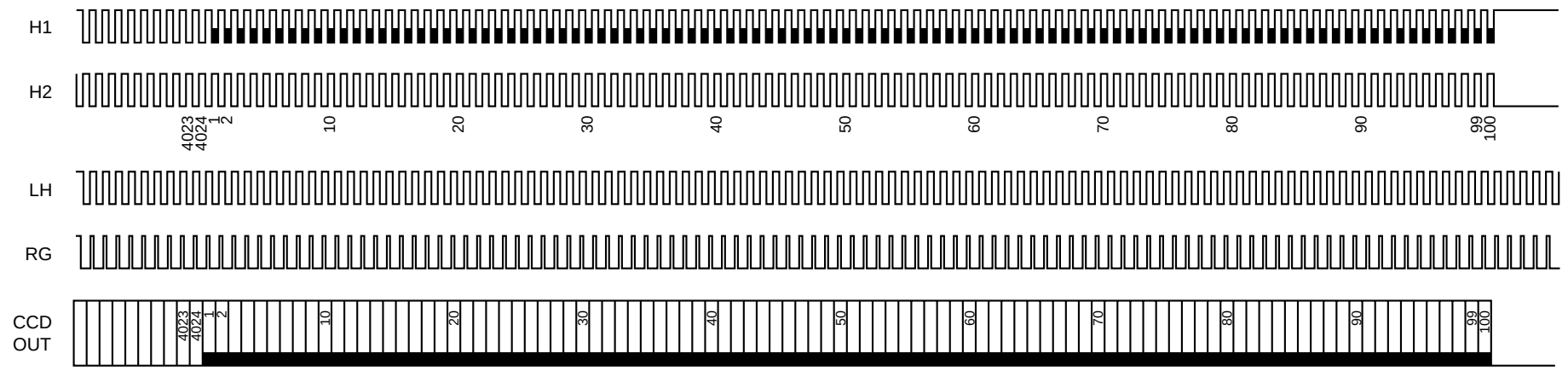
“b1” enlarged



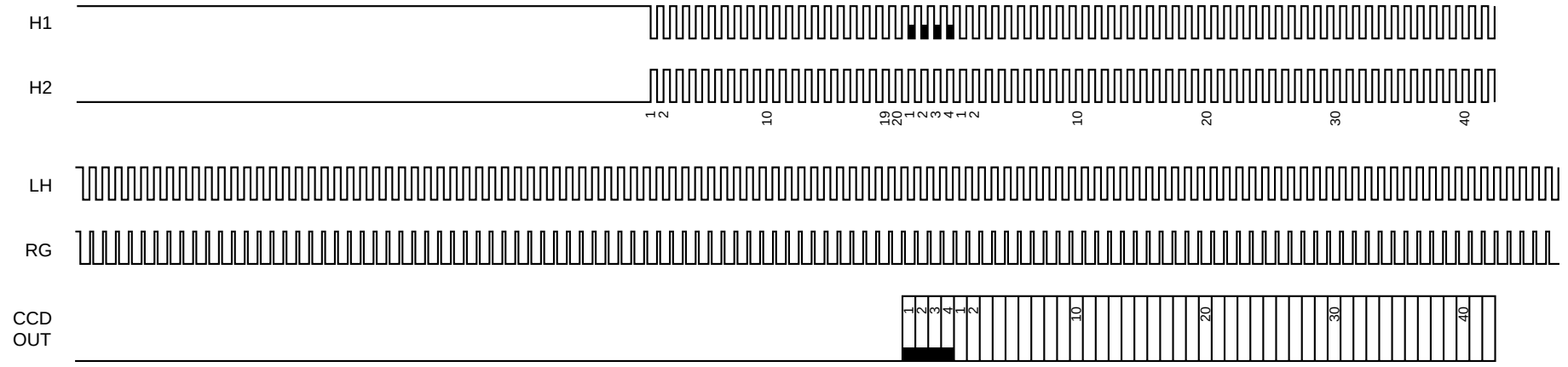
Drive Timing Chart (Horizontal Sync) Frame Readout Mode



Drive Timing Chart (Horizontal Sync “c” Enlarged)

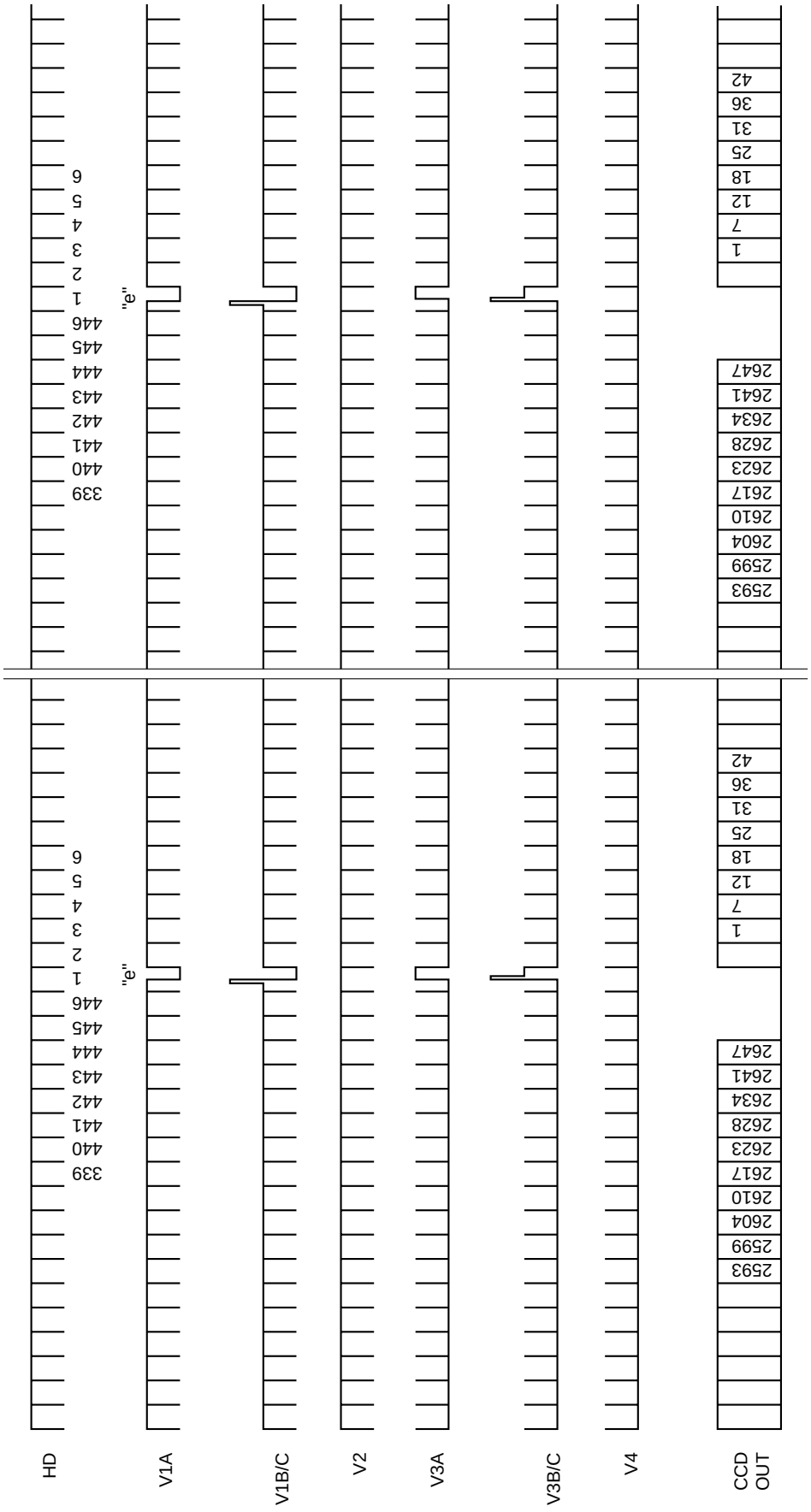


Drive Timing Chart (Horizontal Sync “d” Enlarged)



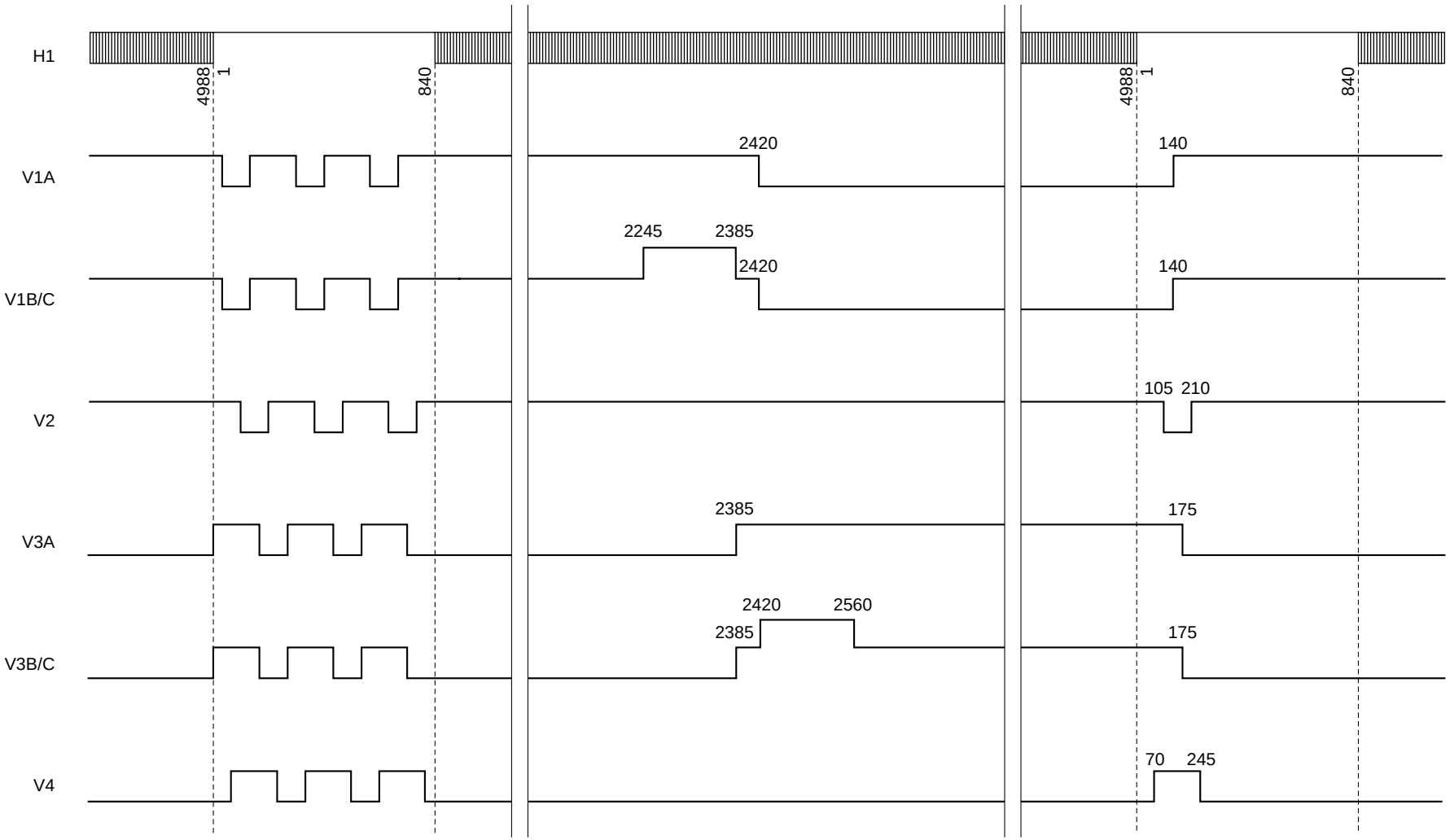
Note) Number of effective horizontal pixels: 4024, number of horizontal optical black pixels: front 4, rear 100, number of horizontal dummy bits: 20

Drive Timing Chart (Vertical Sync) High Frame Rate Readout Mode

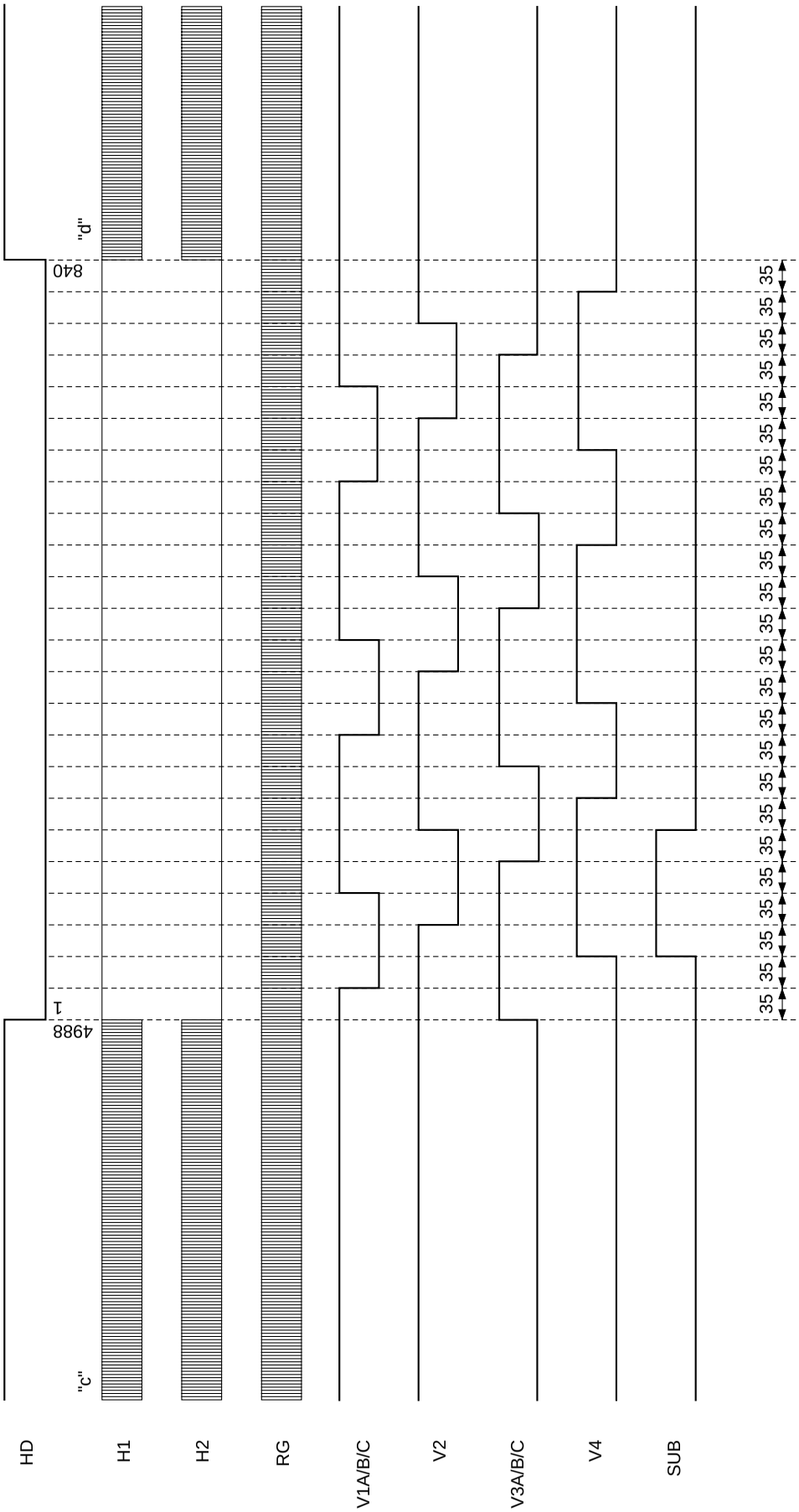


Drive Timing Chart (Vertical Sync) High Frame Rate Readout Mode

(Vertical Sync “e” Enlarged)



Drive Timing Chart (Horizontal Sync) High Frame Rate Readout Mode



Notes on Handling

1) Static charge prevention
   CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.
   a) Either handle bare handed or use non-chargeable gloves, clothes or material. Also use conductive shoes.
   b) When handling directly use an earth band.
   c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
   d) Ionized air is recommended for discharge when handling CCD image sensor.
   e) For the shipment of mounted substrates, use boxes treated for the prevention of static charges.

2) Soldering
   a) Make sure the package temperature does not exceed 80°C.
   b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a ground 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
   c) To dismount an image sensor, do not use a solder suction equipment. When using an electric desoldering tool, use a thermal controller of the zero cross On/Off type and connect it to ground.

3) Dust and dirt protection
   Image sensors are packed and delivered by taking care of protecting its glass plates from harmful dust and dirt. Clean glass plates with the following operation as required, and use them.
   a) Operate in clean environments (around class 1000 is appropriate).
   b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)
   c) Clean with a cotton bud and ethyl alcohol if the grease stained. Be careful not to scratch the glass.
   d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
   e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

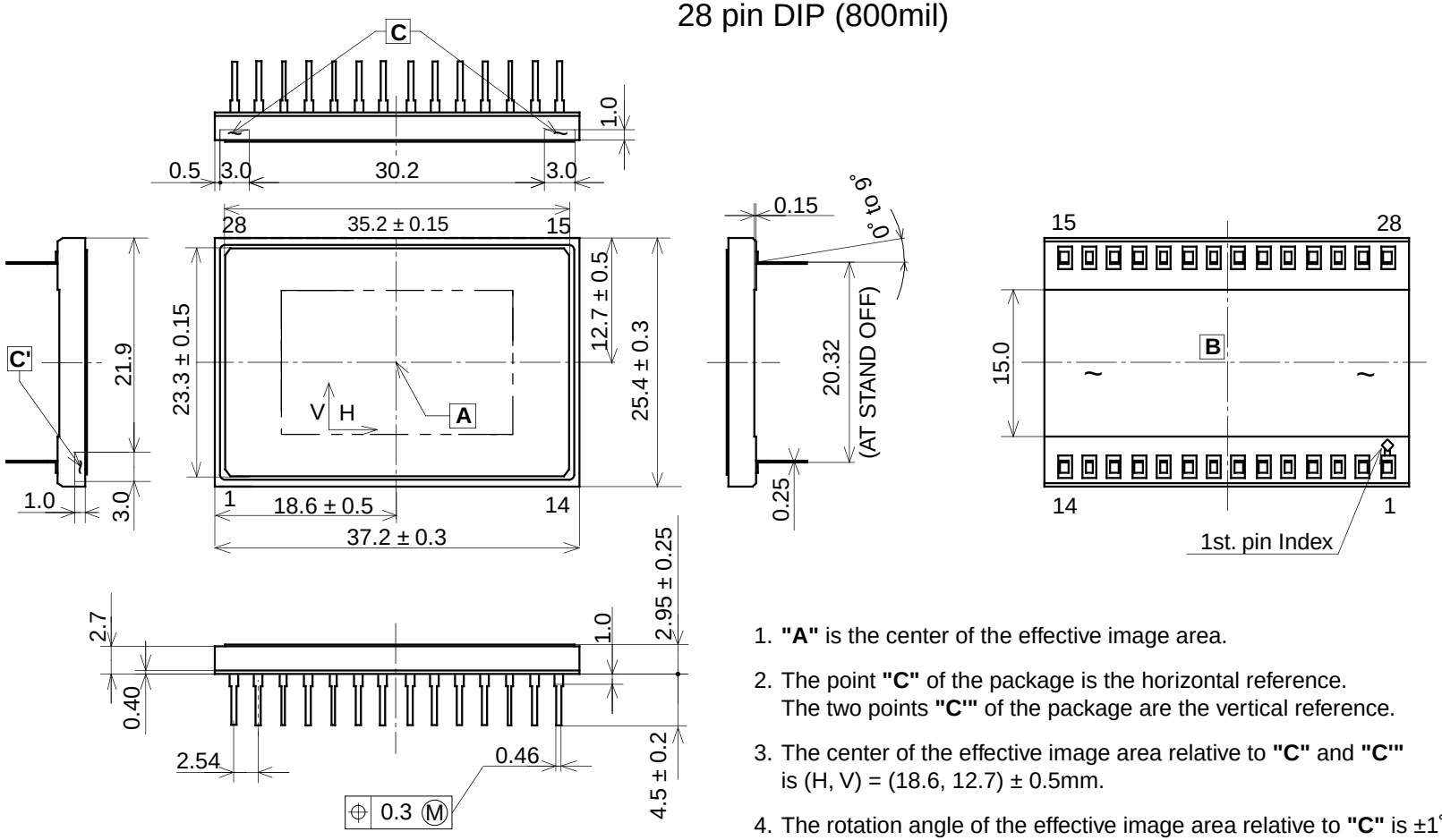
4) Do not expose to strong light (sun rays) for long periods.

5) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensors are precise optical equipment that should not be subject to too much mechanical shocks.

Package Outline Unit: mm

28 pin DIP (800mil)



PACKAGE STRUCTURE

PACKAGE MATERIAL	Ceramic
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	7.80g
DRAWING NUMBER	AS-Z3

1. **"A"** is the center of the effective image area.
2. The point **"C"** of the package is the horizontal reference.
   The two points **"C'"** of the package are the vertical reference.
3. The center of the effective image area relative to **"C"** and **"C'"** is (H, V) = (18.6, 12.7) ± 0.5mm.
4. The rotation angle of the effective image area relative to **"C"** is ±1˚.
5. The height from the reference surface **"B"** to the effective image area is 1.55 ± 0.15mm.
6. The tilt of the effective image area relative to the reference surface **"B"** is 200µm or less.
7. The adhesive must not extend past the cover glass surface.
8. The thickness of the cover glass is 0.75mm (actual dimension), and the refractive index is 1.5.