S5K3C1FX03

(1/3.2” QXGA CMOS Image Sensor)

Preliminary Data Sheet

(Rev 0.12)

DOCUMENT REVISION HISTORY

Versoin	Date	Amendment
0.00	05-11-22	Initial draft for EVT2.
0.01	05-12-08	Reg(0x58, 0x59, 0x68) default values changed.
0.10	05-12-23	DC characteristics changed.
0.11	06-03-03	Description of Single Frame Capture mode is updated.
0.12	06-04-21	Optical format changed from 1/3” to 1/3.2”

Contents

List of Figures

List of Tables

FEATURES

Optical size: 1/3.2 inch
Pixel size: 2.25 um
Effective resolution: 2048 (H) x 1536 (V), QXGA
Line progressive read out
Vertical and horizontal flip mode
Continuous frame capture mode
Sub-sampled readout (x2, x4, x8)
Output format: RAW 8/10/11-bit (10-bit is default)
Max. frame rate: 15fps @ QXGA
Operating temperature: -30°C to +70°C
Supply voltage: 2.8V for analog 1.8V for digital
Internal voltage regulator for 1.5V generation
Internal PLL for high speed clock generation
Internal Scaler for generating lower resolution full field of view image without loss of image quality

GENERAL DESCRIPTION

The S5K3C1FX03 is a highly integrated CMOS image sensor fabricated by SAMSUNG 0.13μm CMOS image sensor process. It is developed for imaging application to realize high-efficiency and low-power photo sensor. The sensor consists of 2048 x 1536 effective pixels which meet with 1/3.2 inch optical format. The sensor has on-chip 11-bit ADC blocks to digitize the pixel output and also on-chip Correlated Double Sampling (CDS) to reduce Fixed Pattern Noise (FPN) drastically. With its few interface signals and 10-bit raw data directly connected to the external devices, a camera system can be configured easily.

PIN DESCRIPTION

Table 1: Chip PAD Description

Pin No	Pin Name	I/O	Description
1	**SCL**	B	CCI clock signal
2	**SDA**	B	CCI data signal
3	**STBYN**	I	Stand-by control signal (active low)
4	**STRB**	I	Control signal for strobe (active high)
5	**REG_CAP**	O	External cap (1uF) connected to DGND
10~19	**D0~D9**	O	Parallel pixel data output. D0 : LSB, D10 : MSB
22	**D10**	O	
23	**PCLK**	O	Pixel clock output
24	**VSYNC**	O	Vertical sync output
25	**HSYNC**	O	Horizontal sync output
26	**SCE**	I	Control signal for test mode. internal pull-down
35	**REF_R**	O	External reference resistor(12kΩ) connected to analog ground
36	**MCLK**	I	External input clock
47	**NC (PLL_FLT)**	O	No Connection (PLL loop filter voltage monitoring)
49	**NC (REF_IN)**	I	No Connection (input for ADC test)
50	**NC (SIG_IN)**	I	No Connection (input for ADC test)
76	**VPAD2**	I	Analog voltage PAD 2. External cap(0.1uF) connected to VSSA
78	**TST2**	I	Control signal for test mode. must connect to VDDA.
79	**TST1**	I	Control signal for test mode. must connect to VSSA.
80	**TST0**	I	Control signal for test mode. must connect to VSSA.
83	**NC (TCLK2)**	I	No Connection (Control signal for test mode. internal pull-down)
84	**NC (TCLK1)**	I	No Connection (Control signal for test mode. internal pull-down)
33,45, 52,74, 82	**VDDA**	P	Analog Power (2.8V)
34,46, 51,75, 81	**VSSA**	P	Analog Ground
6,8,20 ,38,44	**VDDD**	P	Digital Power (1.8V)
7,9,21 ,37,43 ,48,77	**VSSD**	P	Digital Ground

PIN CONFIGURATION

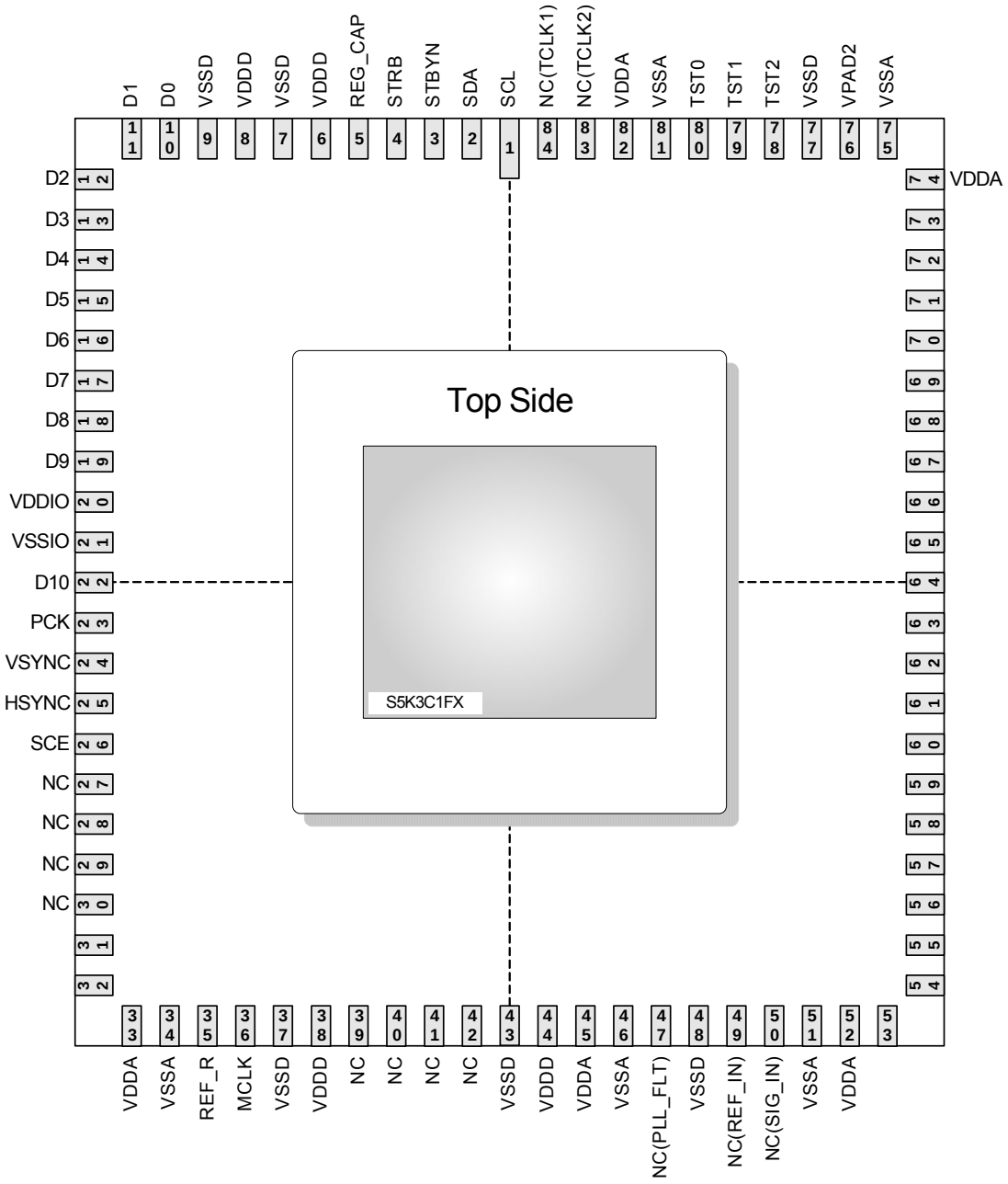


Figure 1: Pin Configuration

PIXEL ARRAY INFORMATION

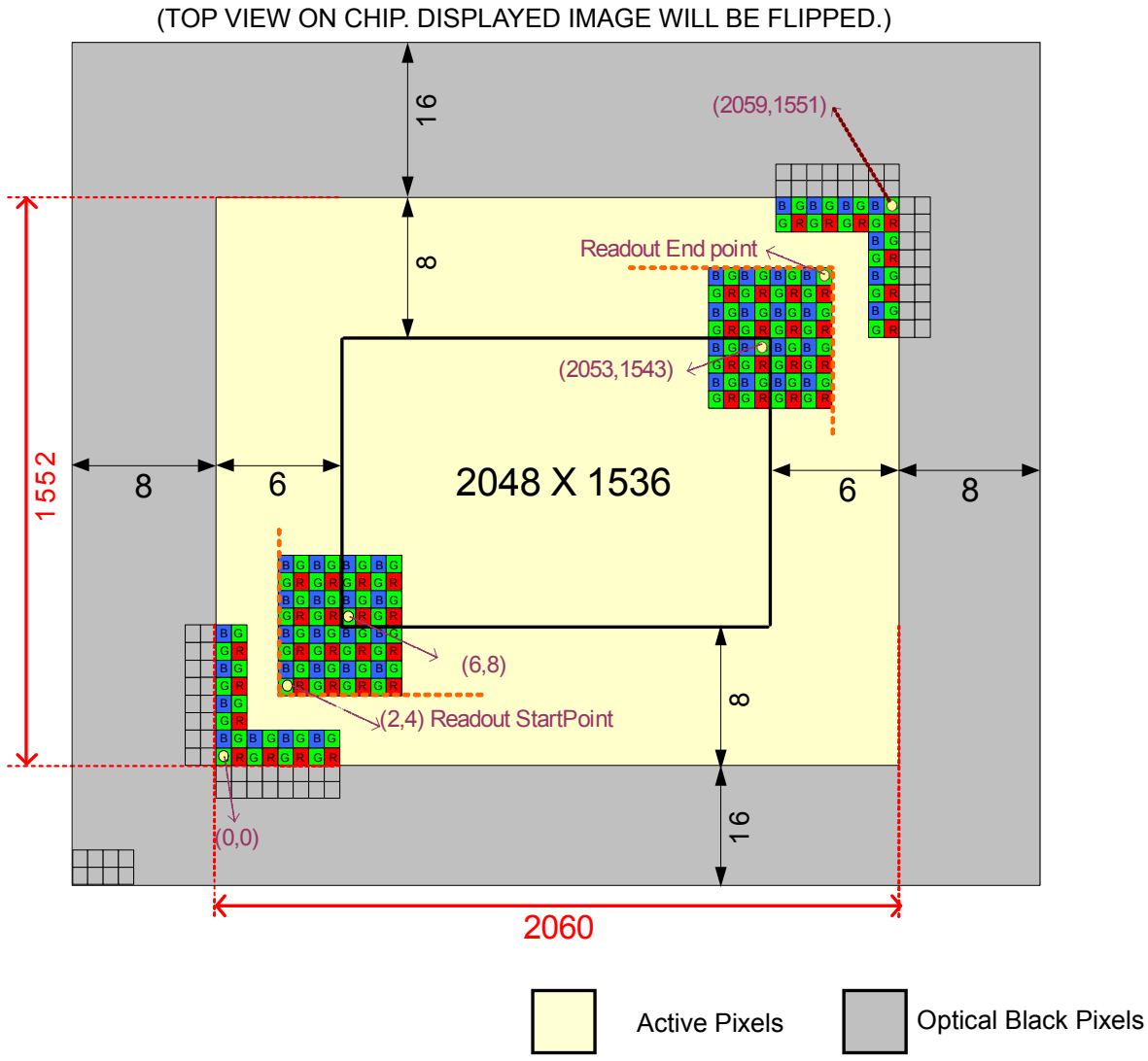


Figure 2: Pixel Array Information

FUNCTIONAL DESCRIPTION

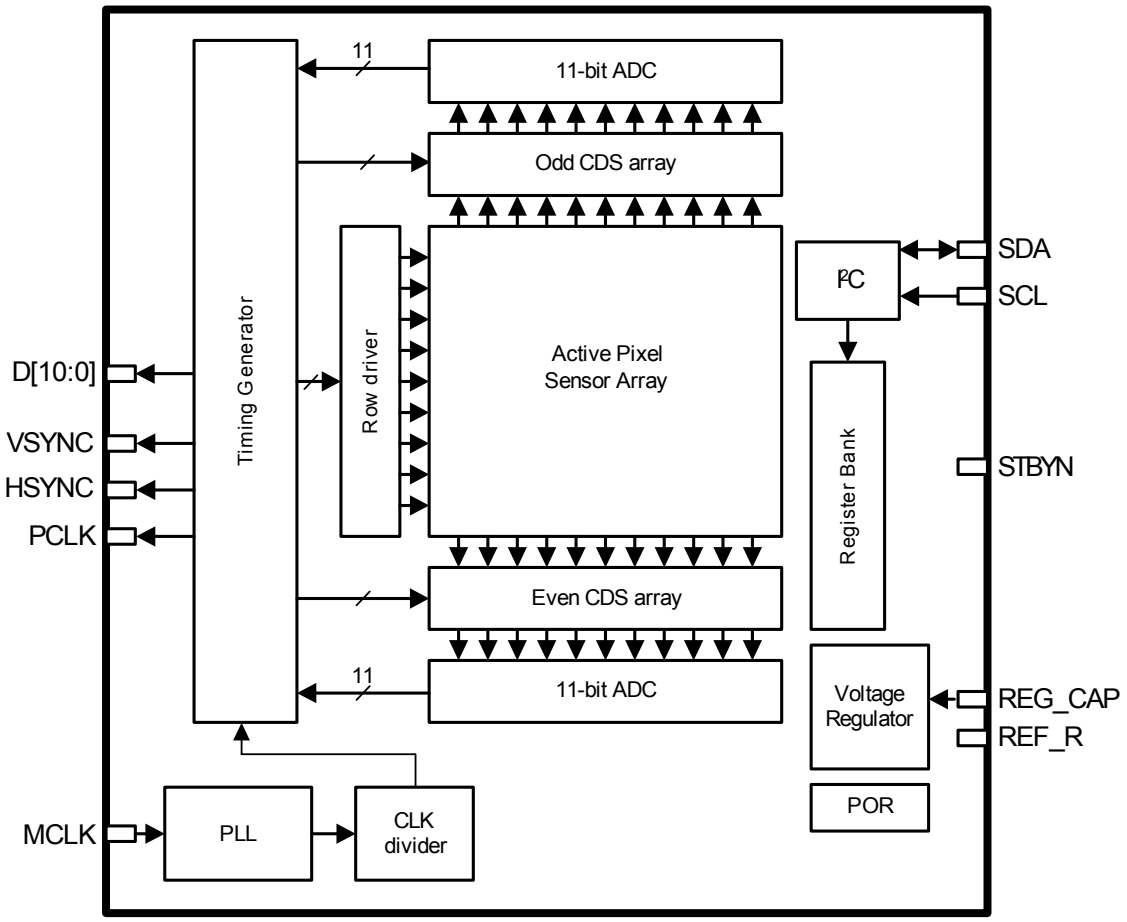


Figure 3: Function Block Diagram

1. Output Data Format

1-1. Synchronous Signal Output

The horizontal sync(HSYNC) and vertical sync(VSYNC) signals are also available. The sync pulse width, polarity and position are programmable by control registers (ref. timing chart). When display mode is enabled, the sync signal outputs indicate that the output data is valid (**hsdisp**=1) or the output rows are valid (**vsdisp**=1).
In default register setting, the output format is RAW 10-bit. the output formats can be selected among RAW 8/10/11-bit by setting **adc_res** register(Bit[3:2] of Reg0x02).

In each output format, the output pin mapping is as follows.

Output format	Output pin	adc_res [3:2]	Description
RAW 8-bit	D10 (MSB) ~ D3 (LSB)	00b	The unused output pins are in low state.
RAW 10-bit	D10 (MSB) ~ D1 (LSB)	01b	
Raw 11-bit	D10 (MSB) ~ D0 (LSB)	10b	

1-2. Pixel array addresses

Addressable pixel array is defined as the pixel address range to be read. The Addressable pixel array can be assigned anywhere on the pixel array. The addressed region of the pixel array is controlled by **x_addr_start**, **y_addr_start**, **x_addr_end** and **y_addr_end** register. Figure 4 refers to a pictorial representation of the Addressable pixel array on the Physical pixel array

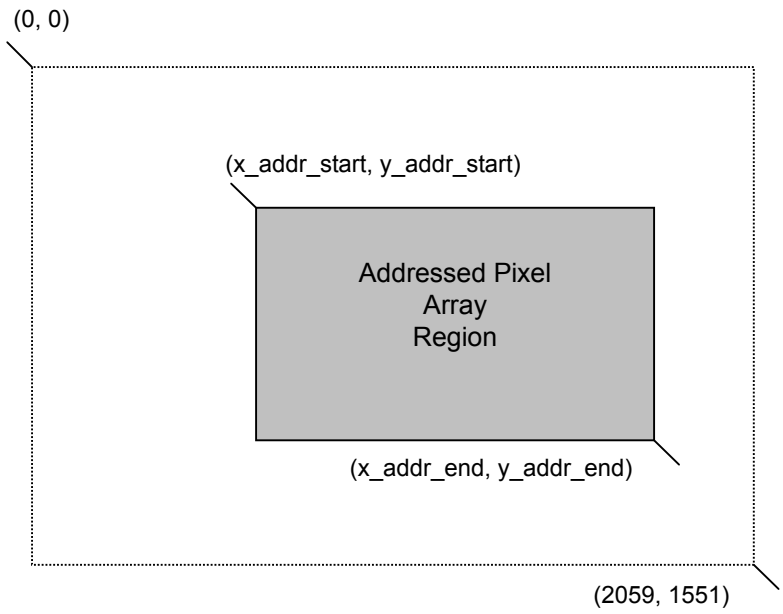
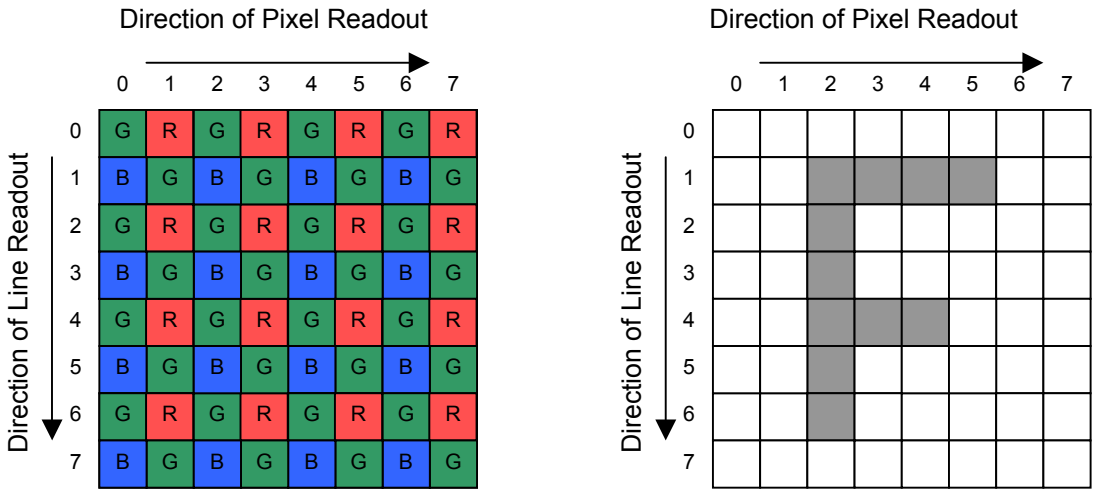


Figure 4: Physical Pixel Array

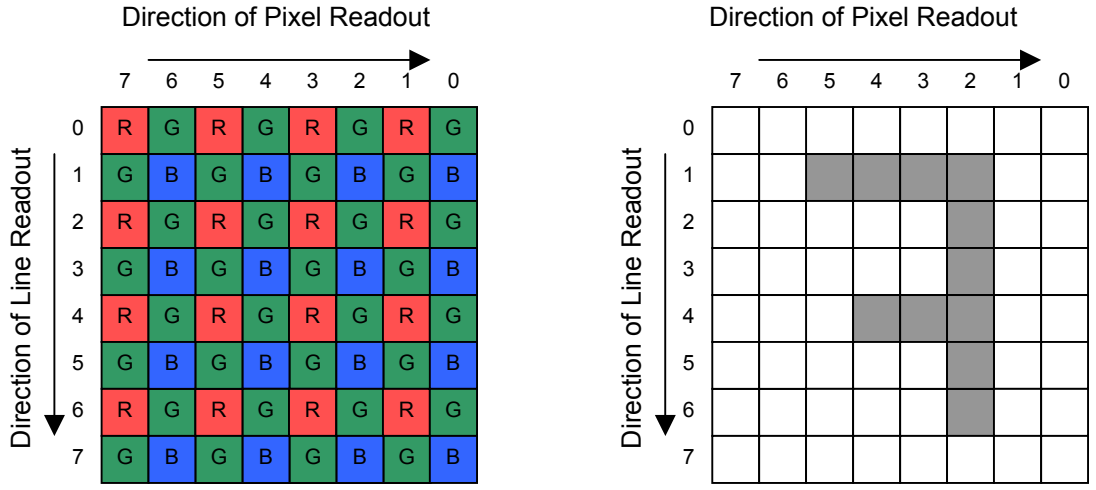
1-3. Mirror/Flip

The pixel data are read out from left to right in horizontal direction and from top to bottom in vertical direction normally. By changing the mirror/flip mode, the read-out sequence can be reversed and the resulting image can be flipped like a mirror image. Pixel data are read out from right to left in horizontal mirror mode and from bottom to top in vertical flip mode. The horizontal mirror and the vertical flip mode can be programmed by image orientation register.
The sensor module support 4 possible pixel readout order

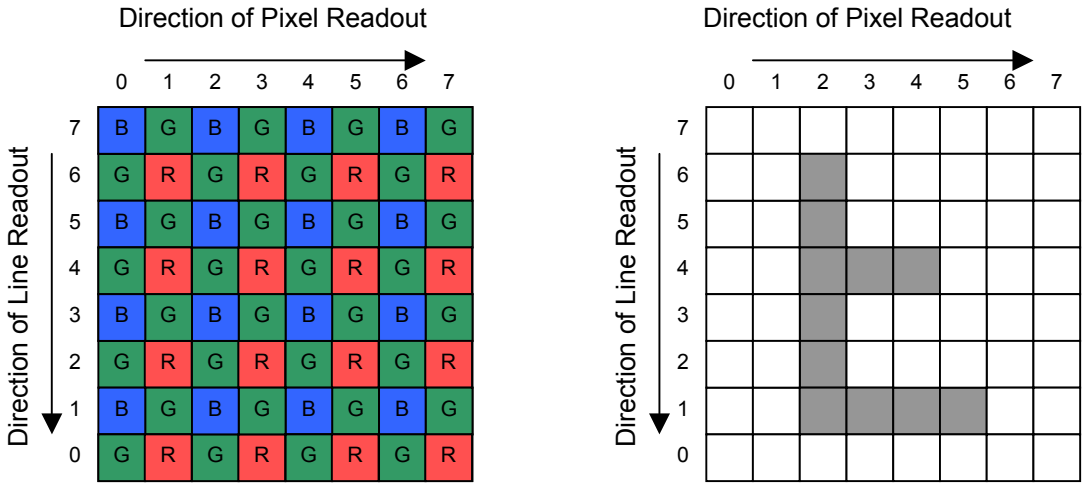
standard readout
Horizontally mirrored readout
Vertical Flipped readout
Horizontally Mirrored and Vertically Flipped readout



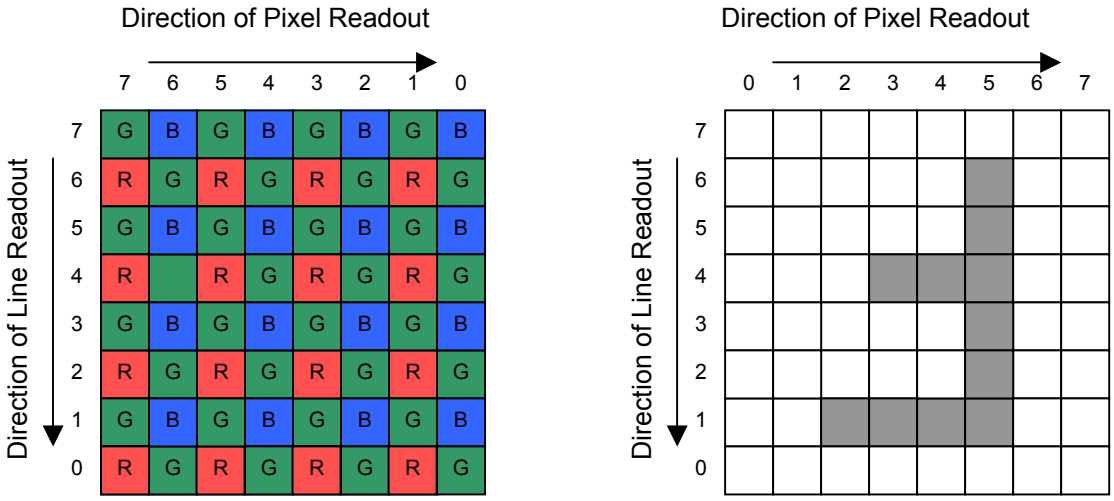
1) Standard Readout



2) Horizontally Mirrored Readout



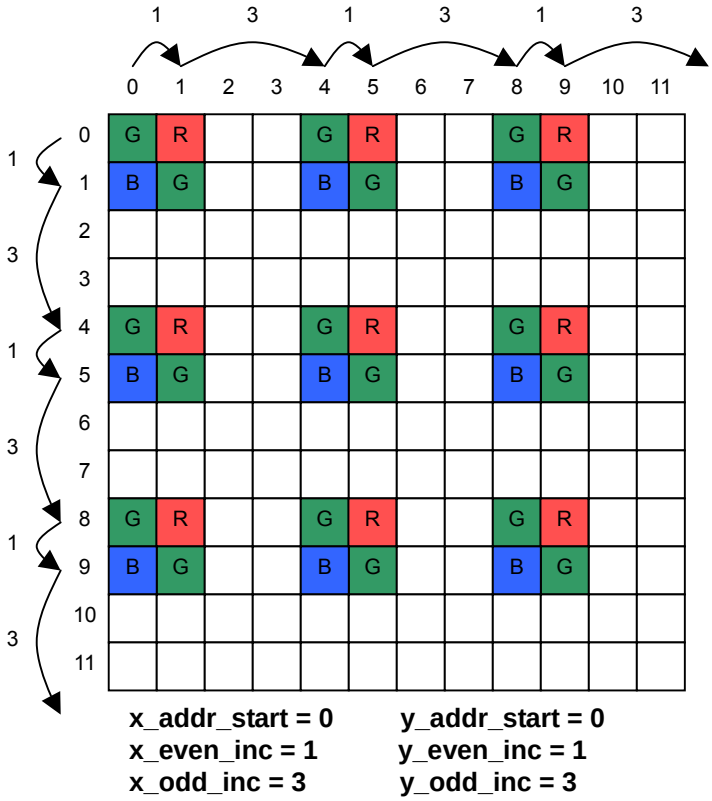
3) Vertically Flipped Readout



4) Horizontally Mirrored and Vertically Flipped Readout

1-4. Sub-Sampled readout

By programming the x and y odd and even increment register (**x_even_inc**, **x_odd_inc**, **y_even_inc**, **y_odd_inc**). the sensor can be configured to readout sub-sampled pixel data.



1-5. Frame Rate Control (Virtual Frame)

The line rate and the frame rate can be changed by varying the size of virtual frame. The virtual frame's width and depth are controlled by **line_length_pck** and **frame_length_lines** register. The frame rate can be calculated by the following equation:

Frame rate = 1 / (line_length_pck * frame_length_lines) * DCLK

For S5K3C1FX03, the minimum **line_length_pck** is 2488(decimal) and other parameters can be set appropriately according to the above equation.

1-6. Integration Time Control (Electronic Shutter Control)

The pixel integration time is controlled by shutter operation. In shutter operation, the amount of time, integration time, is determined by the column Step Integration Time Control Register (**fine_integration_time**) and line Step Integration Time Control Register(**coarse_integration_time**). The total integration time of sensor module can be calculated using the following formula.

Total_integration_time =
{(coarse_integration_time*pixel_period_per_line)+fine_integration_time} * 1/DCLK

1-7. Continuous Frame Capture Mode(CFCM) Integration Time Control (Electronic Shutter Control)

In CFCM operation, the integration time is controlled by shutter operation. The shutter operation is done when shutter control register (**shut_ctrl**) is set to "1". In shutter operation, the integration time is determined by the Row Step Integration Time Control Register(**coarse_integration_time**) and Column Step Integration Time Control Register(**fine_integration_time**).

2. Analog to Digital Converter (ADC)

The image sensor has an on-chip 11-bit ADC. Column parallel ADC scheme is used for low power analog processing. The default ADC resolution is 10-bit and D10 to D1 are used to output image data parallelly.

2-1. Correlated Double Sampling (CDS)

The analog output signal of each pixel includes some temporal random noise caused by the pixel reset action and some fixed pattern noise by the in-pixel amplifier offset deviation. To eliminate those noise components, a correlated double sampling(CDS) circuit is used before converting to digital. The output signal sampled twice, once for the reset level and once for the actual signal level sampling.

2-2. Analog Gain and Offset Control

The user can control the gain of pixel signal by analog gain control registers(**analogue_gain_code_greenR**, **analogue_gain_code_red, analogue_gain_code_blue, analogue_gain_code_greenB)** and offset by offset control registers (**offset_gr, offset_r, offset_b, offset_gb**). Global analog gain can be set using analog gain con (**analogue_gain_code**).
the analog gain can be given by the following equation:

$$\text{Analog Gain} = (m_0 \times + c_0) / (m_1 \times + c_1)$$

S5K3C1FX03 specifies analog gain by coefficients of $m_0 = 0$, $c_0 = 128$, $m_1 = -1$, $c_1 = 128$. As a result, users can control analog gain as following equation:

$$\text{Analog Gain} = 128 / (128 - \textbf{analogue\_gain\_code}\ [7:0])$$

Separate channel gain is also supported in addition to global analog gain. Theoretically, maximum x128 gain can be obtained, but analog gain up to x8 is recommended for image quality.

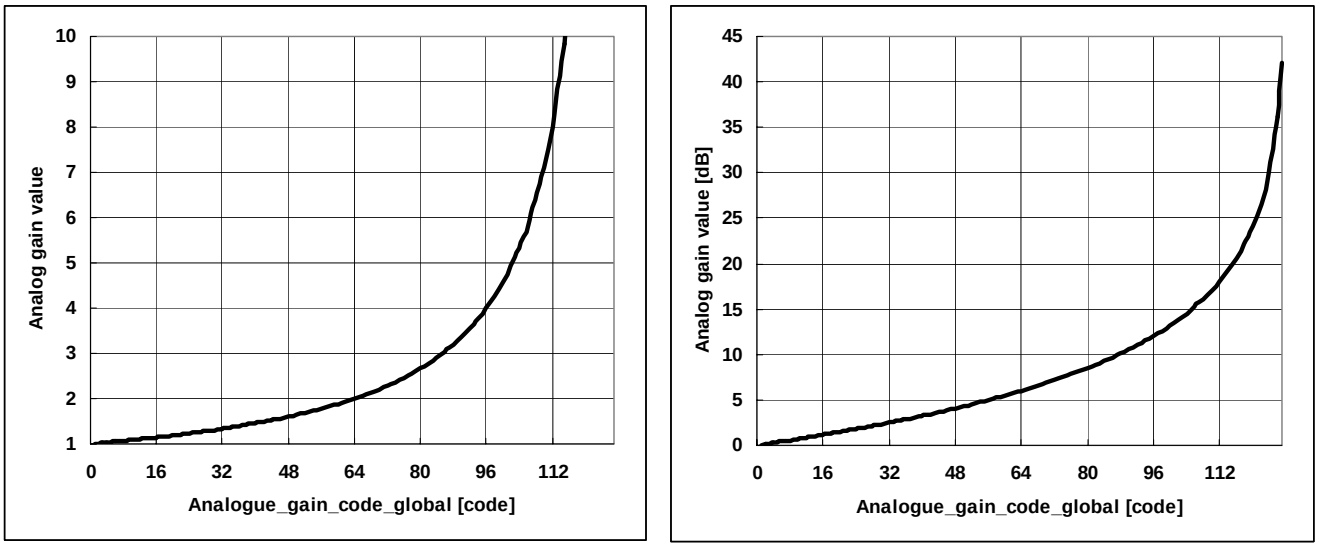


Figure 5: Analog Gain Value

2-3. Quadrisectional Global Gain Control

The user can controls the global gain to change the gain for all color channels by the Global Gain Control Registers (global_gain_sec1, global_gain_sed2, global_gain_sec3, global_gain_sec4). The global gain control register is composed of four register groups and each register value decides the gain for each quarter section of output code level.
By appropriately programming these four register values, the different output resolution according to the signal can be achieved and the intra-scene dynamic range can be increased by 16 times. In another application, the sectional global gain control can be used as a rough gamma correction with four sectional linear approximation curve as shown in figure 7. (**ggs** is acronym of **global_gain_sec**)

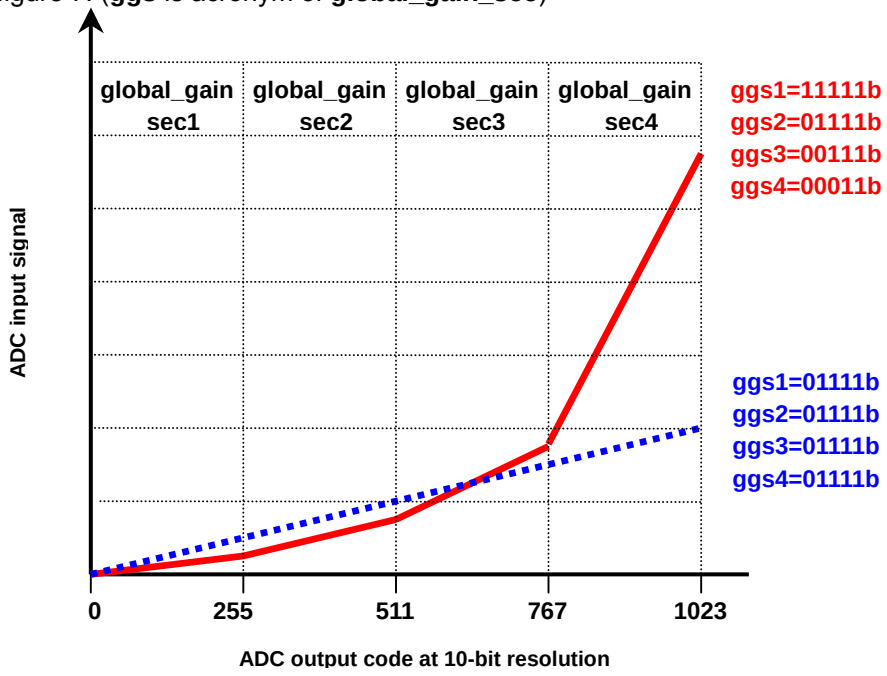


Figure 6: Quadrisectional Global Gain Control

3. POST PROCESSING

3-1. Dark Level Compensation

The dark level of Image sensor is defined as average output level without illumination. It includes pixel output caused by leakage current of the photodiodes and ADC offset. To compensate the dark level, the output level of optical black(OB) pixels can be a good reference value. When Auto Dark Level Compensation Register (**fadlc_en**) is set, the image sensor detects the OB pixel level at the start of every frame and analog-to-digital conversion range is shifted to compensate the dark level for that frame. So, the resulting output data of that frame will be almost zero under dark state. If user wants the dark level which is not zero, the ADC Offset Register (**even_cnt_del**, **odd_cnt_del**) can be used. The lower 7-bit value represent the offset value in output code for compensation and the MSB is the sign to define whether the offset is positive (**even_cnt_del**[7], **odd_cnt_del**[7]=0) or negative(**even_cnt_del**[7], **odd_cnt_del**[7]=1). When not in auto dark level compensation mode, the **even_cnt_del**[7:0], **odd_cnt_del**[7:0] act as a output code value to subtract the output image data. Please notify that the all the 8-bit data are used for an offset value without sign bit.

ADLC formula : Dfinal = D(n) + **even_cnt_del**[7:0] (**odd_cnt_del**[7:0])
D(n) = (gain_a)*(OB(n) + OB(n-1)) + (gain_b)*D(n-1)

4. I²C SERIAL INTERFACE

4-1. IIC Bus Overview

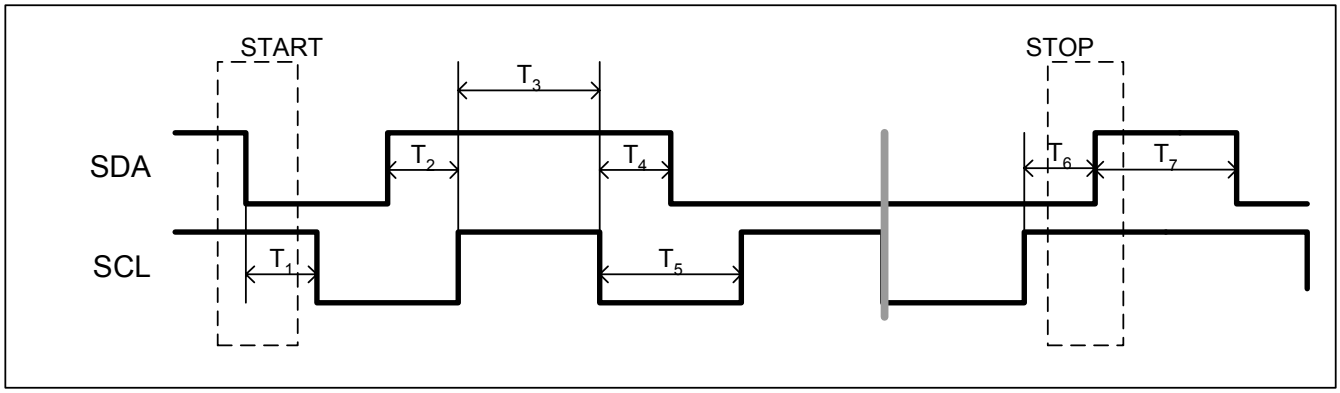
The IIC contains a serial two-wire (half duplex) interface that features bi-directional operation, master or slave mode. The general SDA and SCL are the bi-directional data and clock pins, respectively. These pins are open-drain type ports and will require a pull-up resistor to VDD. The SDA bus line may only be changed while SCL is low. The data on the SDA bus line is valid on the high-to-low transition of SCL.

4-2. Protocol

The IIC bus interface is composed of following parts. START signal, 7-bit slave device address (0010001b) transmission followed by a read/write bit, an acknowledgement signal from the slave, 8-bit data transfer followed by an acknowledgement signal and STOP signal.

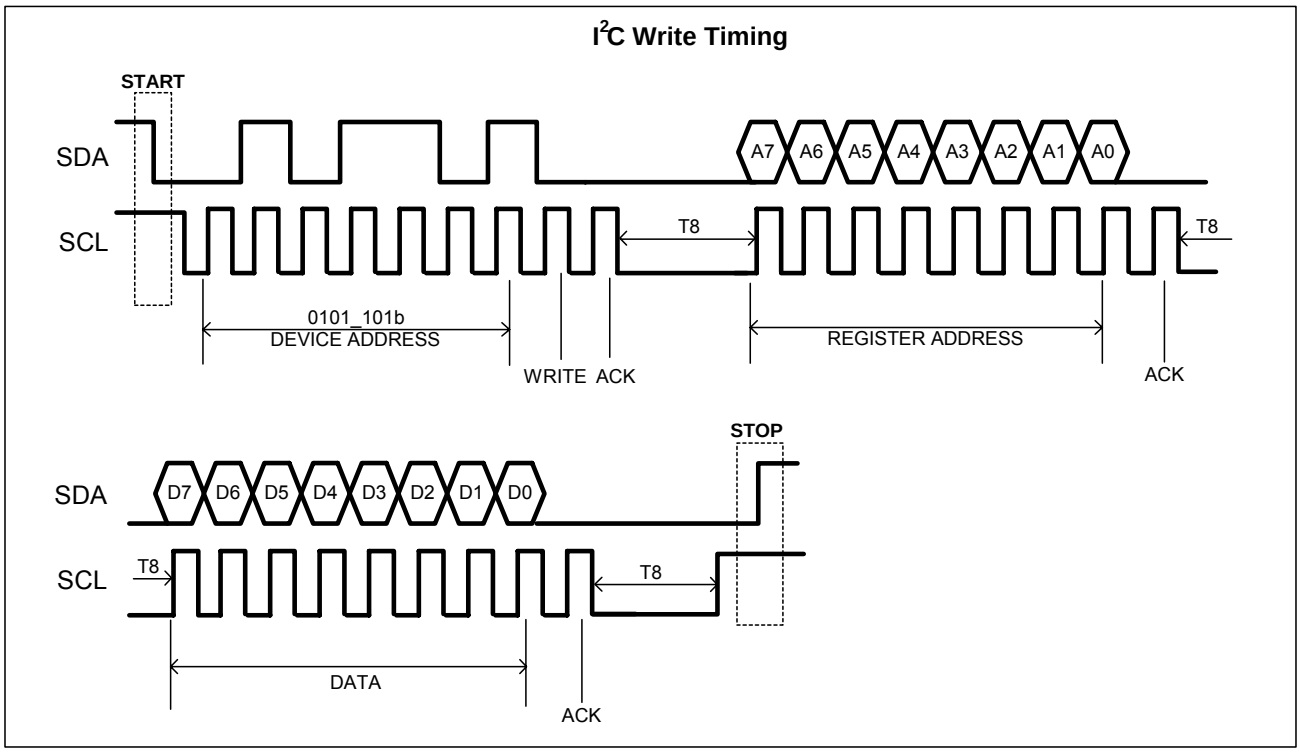
4-3. Notice & Usage

The S5K3C1FX03 internal registers have several pages to expand its address space. Our host interface uses only 8-bit data to assign a register, thus a page setting must be required in advance and its selected page will be kept until changed.



SYMBOL	PARAMETER	MIN	MAX	UNIT
	SCL clock frequency	-	400	KHz
T1	Hold time for START condition	0.6	-	us
T2	Data setup time	100	-	ns
T3	High period of the SCL clock	0.6	-	us
T4	Data hold time	10	-	ns
T5	Low period of the SCL clock	1.3	-	us
T6	Setup time for STOP condition	0.6	-	us
T7	Bus free time between a STOP and START condition	1.3	-	us

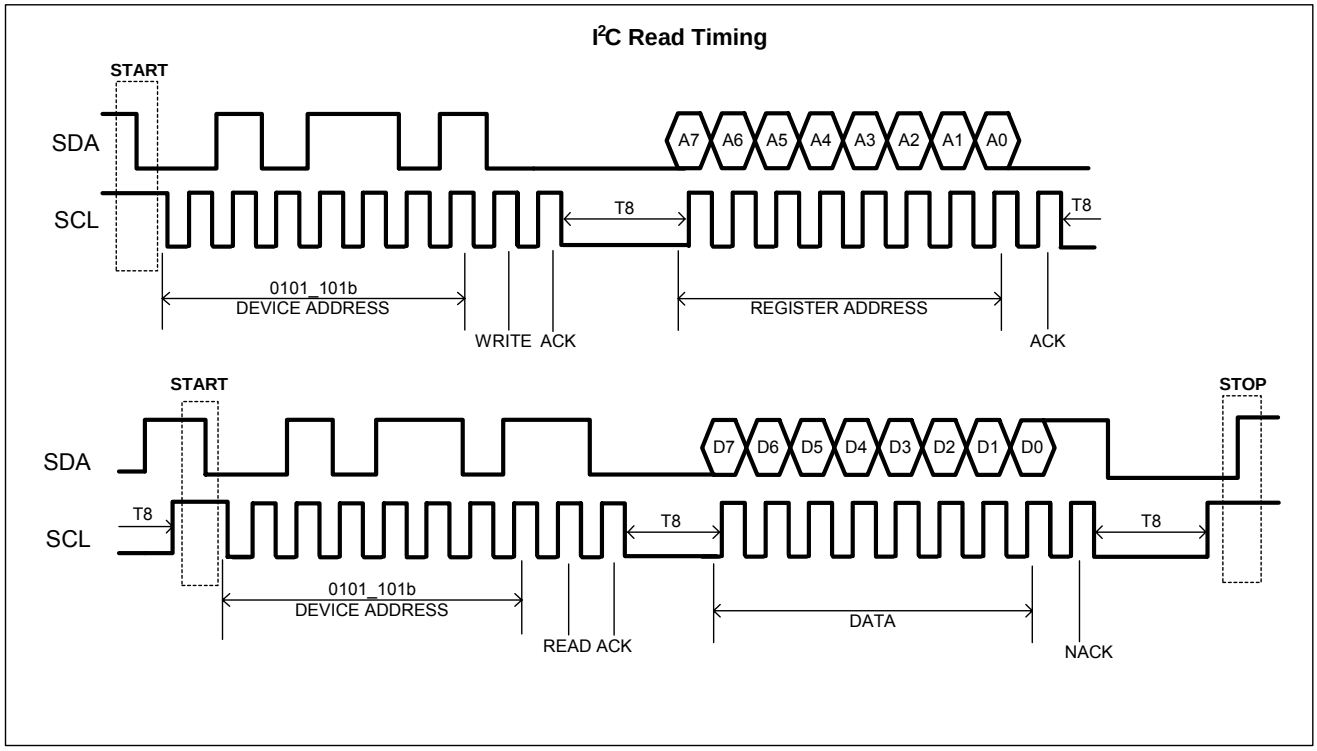
Figure 7: IIC General Timing



SYMBOL	PARAMETER	MIN	MAX	UNIT
T8	Minimum required time for slave Interrupt processing	150	-	cycle

[NOTE]
(1) cycle: MCLK cycle time

Figure 8: IIC Write Timing



SYMBOL	PARAMETER	MIN	MAX	UNIT
T8	Minimum required time for slave Interrupt processing	150	-	cycle

[NOTE]
(1) cycle: MCLK cycle time
(2) A repeated START is required

Figure 9: IIC Read Timing

5. PLL and Clock Generator

S5K3C1FX03 contains a Phase-Locked Loop(PLL) and a clock generator, which generates all the necessary video timing and output pixel clocks from the external clock of 6 ~ 27MHz. By setting pre PLL clock divider(**pll_p**), PLL multiplier(**pll_m**) and clock dividers(**dck_div1&2, pck_div1&2**) appropriately, users can get necessary clock frequency.
The overall clock tree structure is shown in Figure 11, and there are shown user-controllable divide-ratios.
The necessary frequencies are synthesized by the following equations.

PLL input clock = external input clock / pre PLL clock divider
PLL output clock = PLL input clock * PLL multiplier
Data clock (DCK) = PLL output clock / (DCK clock divider 1 * DCK clock divider 2)
Pixel clock (PCK) = PLL output clock / (PCK clock divider 1 * PCK clock divider 2)

Using the external clock frequency of 13 MHz and default register setting, the data and pixel clock frequency is 32.5MHz.

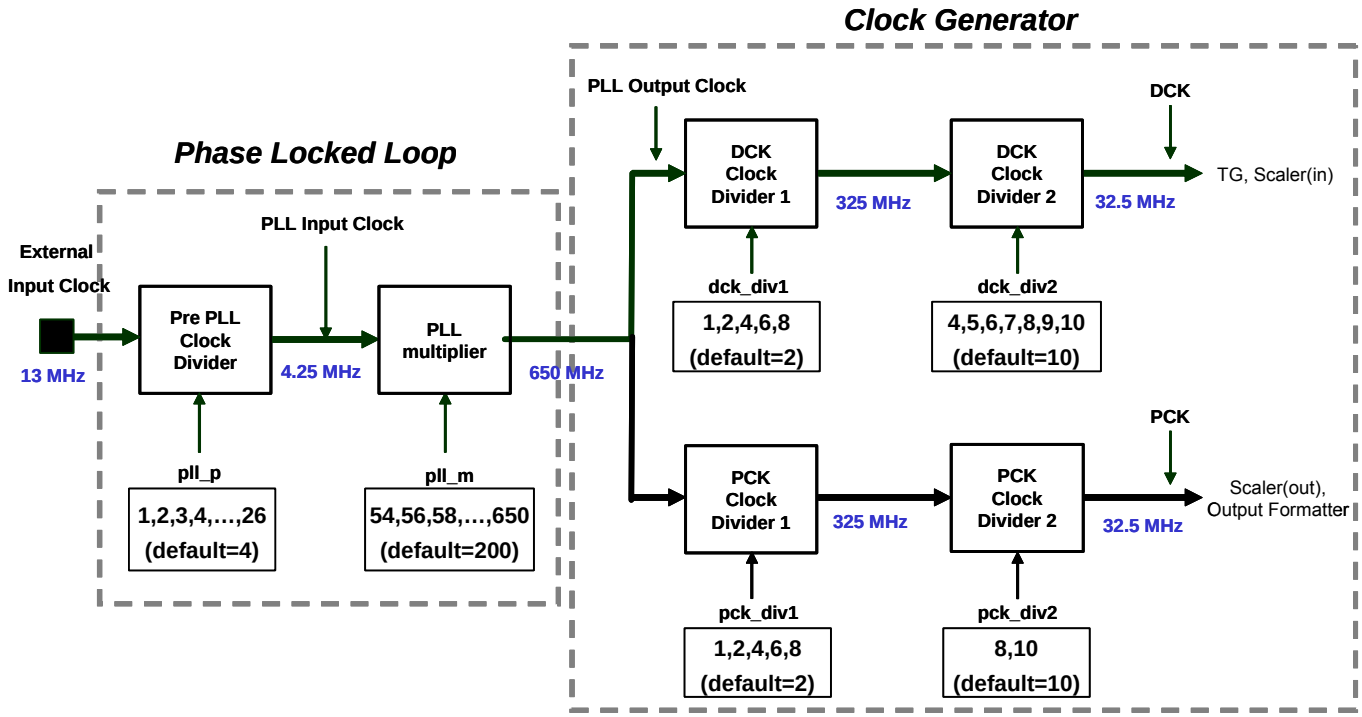
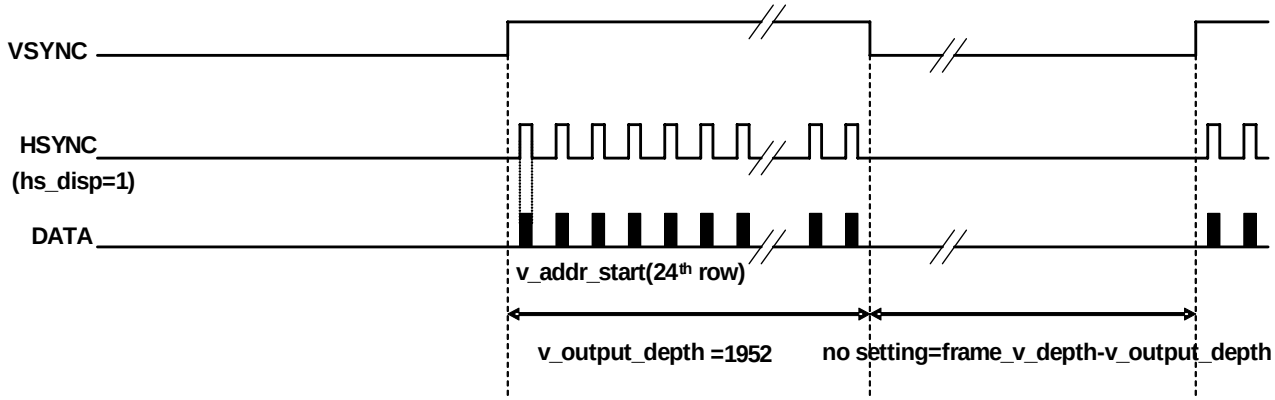


Figure 10: Clock tree structure

VERTICAL TIMING DIAGRAM

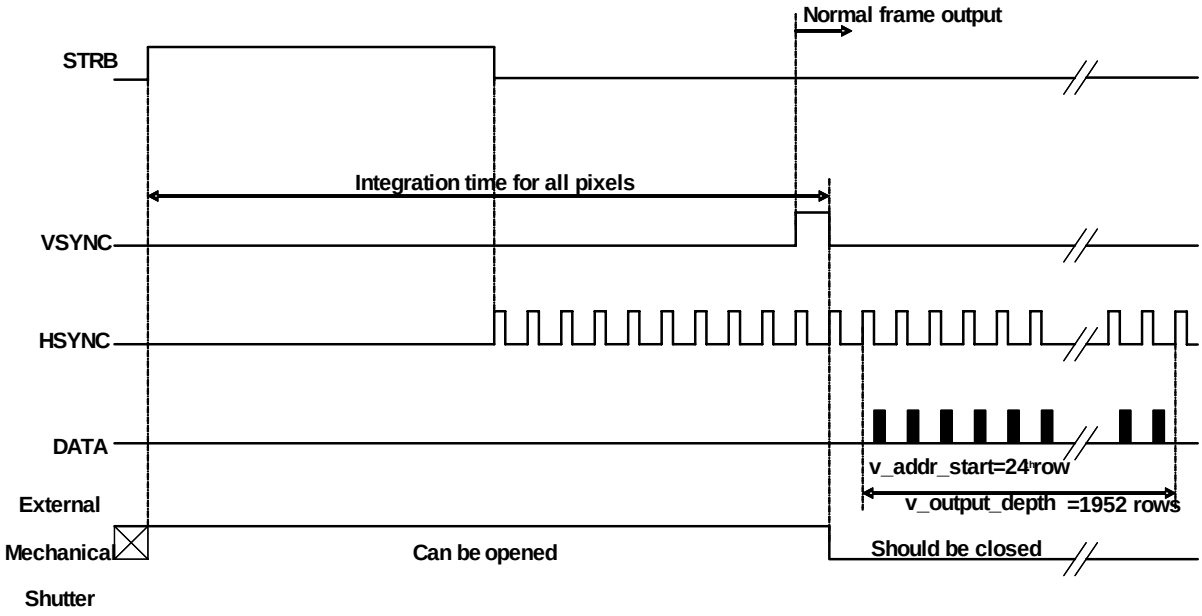
Continuous Frame Capture Mode

(Vertical Data Valid Mode Case) vs_disp=1



Vertical Timing Diagram (CONTINUED)

Single Frame Capture Mode
(Mechanical Shutter Case mech_mod = 1)



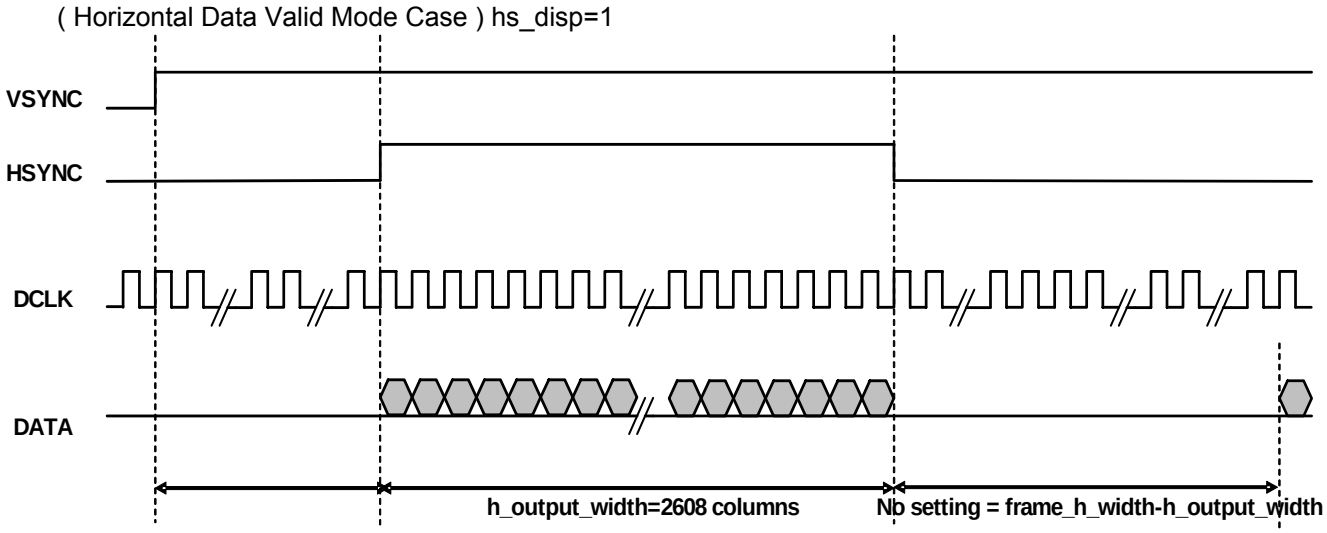
About Single Frame Capture Mode.
Single Frame Capture Mode can capture only one frame. Using this mode, user follows belowing step.

1. Set register mech_mod<02h,[6]> to 1.
2. Sensor meet end of frame. It wait STRB(External Input) signal.
3. Let STRB(External Input) to high. Within this time pixel integrate charge.
4. Let STRB to low. Sensor prepare to display.
5. 12 Hsync past, Sensor display Image DATA.

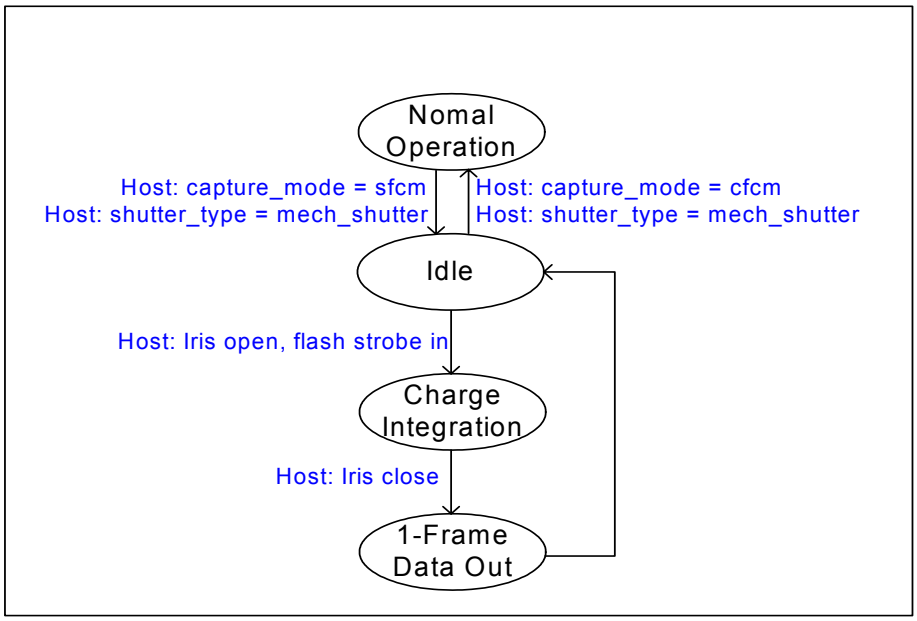
About Mechanical Shutter Operation

1. Within STRB signal is high, Iris of Mechanical Shutter must open to gether light to pixel.
2. After Vsync, Iris of Mechanical Shutter must close to block light.

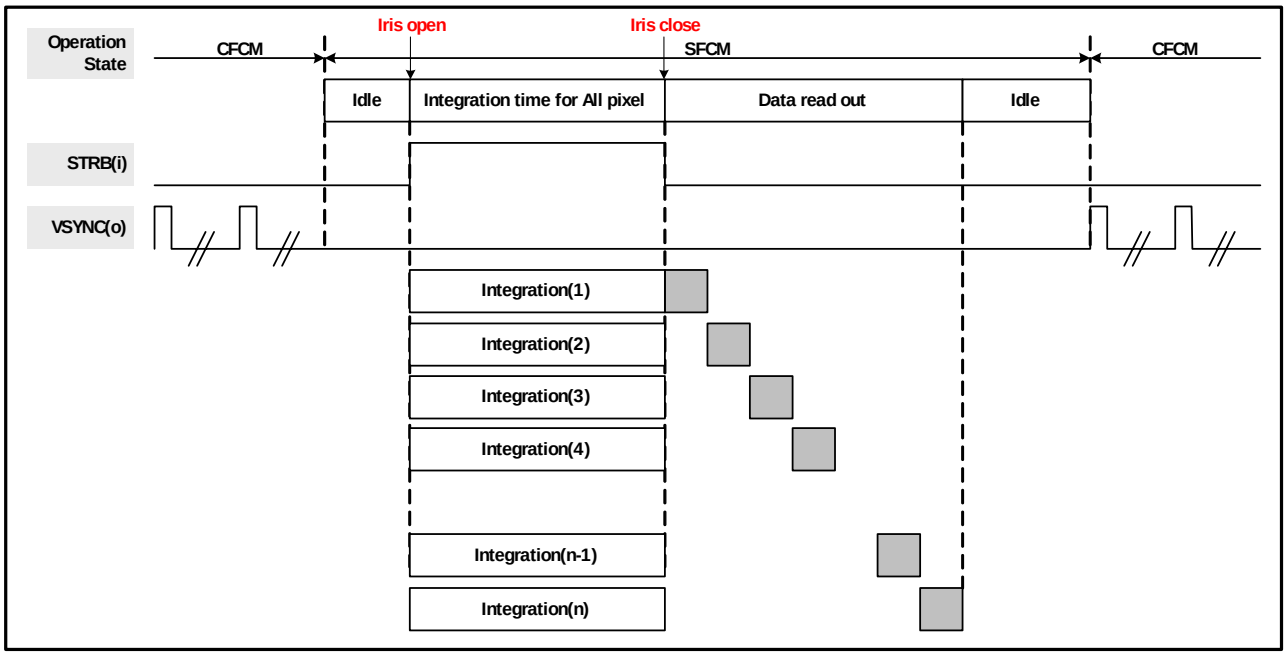
HORIZONTAL Timing Diagram



MECHANICAL SHUTTER OPERATION



Mechanical Shutter Operation Scenario



SFCM Operation Timing with Mechanical shutter

POWER UP/DOWN SEQUENCE

The digital and analog supply voltages can be powered up in any order e.g. VDDD then VDDA or VDDA then VDDD.

On power up :

- If STBYN is low when the power supplies are brought up then the sensor will go into power-down mode.
- If STBYN is high when the power supplies are brought up then the sensor will go into software stand-by mode

In both cases the presence of an on-chip power-on reset cell ensures that the internal register values are initialized correctly to their default values. The MCLK clock can either be initially low and then enabled during stand-by mode or MCLK can be a free running clock.

As shown in Figure 12, the operation state is composed of 3 modes which are power-down, stand-by and active operation modes.
During the power-down mode where external power supplies are applied and STBYN is in low state, sensor does not operate and the current consumption of power supplies are nearly zero. In this operation mode, all I^2C registers are reset to their defaults values. During the stand-by mode where STBYN is switched to high state, the current consumption of power supplies are minimized and I^2C communication is possible. The clock divider and PLL multiplier registers must be configured during stand-by mode while PLL is powered down. Sensor enters active operation mode by setting **streaming** register (Bit[4] of Reg0x03h) to 1b where pixel data is output through D10 ~ D0 pins.

The power down sequence is the reverse order of power up sequence, i.e., active operation mode → stand-by mode → power down mode.

Table 2: Power-Up Sequence Timing Constraints

Constant	Label	Min	Max	Units
VDDA rising – VDDD rising	t0	VDDA and VDDD may rise in any order. The rising separation can vary from 0ns to indefinite		ns
VDDD rising – VDDA rising	t1			ns
VDDA rising – STBYN rising	t2	0.0		ns
STBYN rising – First I^2C transaction	t3	15us + 16 MCLK Cycles		
Minimum No. of MCLK cycles prior to the first I2C transaction	t4	16		MCLK cycles

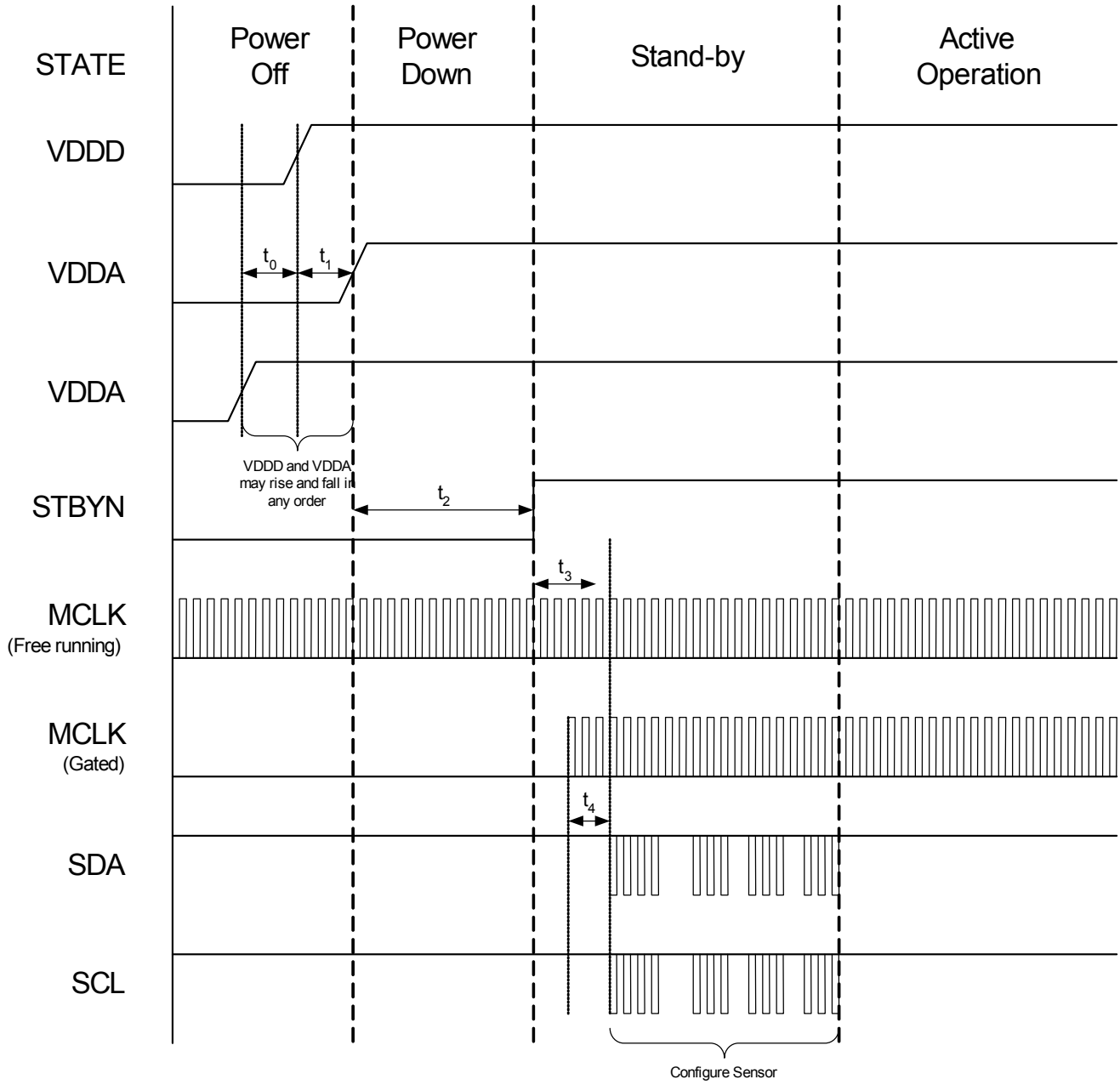


Figure 11 : Power-Up Sequence

ELECTRICAL CHARACTERISTICS

Table 3: Absolute Maximum Rating

Symbol	Description	Min	Typical	Max	Units
VDDD	Digital Absolute Max (1)	-0.3		2.2	V
VDDA	Analogue Absolute Max (2)	-0.3		4	V
$V_{IP(DIG)}$	Digital Input Voltages (3)	-0.3		VDDA+0.3	V
T_{STR}	Storage Temperature	-40		85	°C

[Notes:]
(1) Digital Supply 1.9V + 0.3V
(2) Analogue Supply 2.9V + 0.3V
(3) Digital Inputs: MCLK, STBYN, SCL, SDA, SCE, TST0, TST1, TST2

Table 4: DC Characteristics

(T_A = -30 to +70°C, C_L = 15pF)

Characteristics	Symbol	Condition	Min	Typ	Max	Unit
Operating voltage	V_{DDH}	applied to VDDA pins	2.55	2.8	3.05	V
	V_{DDL}	applied to VDDD pin	1.65	1.8	1.95	
	VDDIO	Applied to VDDIO pin	1.65		3.05	
Input voltage(1)	V_{IH}	-	0.7*VDDIO	-	2.8	
	V_{IL}	-	-	-	0.2*VDDIO	
Input leakage current(2)	I_{IL}	V_{IN} = V_{DDL}	-10	-	10	μA
Input leakage current with pull-down(3)	I_{ILD}	V_{IN} = V_{DDL}	5	20	50	
High level output voltage(4)	V_{OH}	I_{OH} = -4mA(4)	VDDIO-0.2	-	-	V
		I_{OH} = -4mA(5)	VDDIO-0.2	-	-	
Low level output voltage(5)	V_{OL}	I_{OL} = 4mA(4)	-	-	0.2	
		I_{OL} = 4mA(5)	-	-	0.2	
High-Z output leakage current(6)	I_{OZ}	V_{OUT} = GND or VDDIO	-10	-	10	μA
Input capacitance(1)	C_{IN}	-	-	-	4	pF
Supply current	I_{STBL}	STBYN=Low(Active) All input clocks = Low 0 lux illumination applied to VDDD pin	-	-	10	μA
	I_{STBH}	STBYN=Low(Active) All input clocks = Low 0 lux illumination applied to VDDA pin	-	-	10	μA
	I_{DDL}	f_{DCLK} = 32.5MHz 0 lux illumination applied to VDDD pin	-	40	50	mA
	I_{DDH}	f_{DCLK} = 32.5MHz 0 lux illumination applied to VDDA pin	-	40	50	mA

NOTES:

1. Applied to MCLK, STBYN, SCL, SDA, SCE, TST0, TST1, TST2 pins.
2. Applied to MCLK, STBYN, SCL, SDA, TST0, TST1, TST2 pins
3. Applied to SCE pin
4. Applied to SCL and SDA pin
5. Applied to PCLK, HSYNC, VSYNC, D0 to D10, SCL, SDA pin
6. Applied to PCLK, HSYNC, VSYNC, D0 to D10 pin when in High-Z output state

Table 5: Imaging Characteristics

(All the values are obtained by using the SMIA 1.0 characterization method. Electrical operating conditions follow the recommended typical values : VDDA=2.8V, VDDD=1.8V, T_A = 23°C, analog_gain = 1x for most of items except for PSRR.)

Characteristics	Min	Typ	Max	Unit
Light Test				
Sensitivity		0.067		1/Cdm $^{-2}$.sec
Photo Response Non-Uniformity		1.14		%
Module Response Non-Linearity (INL) (1)		0.0033		Code/FSD
Module Response Non- Linearity (DNL) (1)		0.0760		Code/FSD
SNR at 10 Cdm $^{-2}$		36.72		dB
SNR at 50 Cdm $^{-2}$		37.48		dB
SNR at 100 Cdm $^{-2}$		37.54		dB
SNR at 450 Cdm $^{-2}$		37.58		dB
Maximum illumination		1041800		Cdm $^{-2}$
Minimum illumination		0.224424		Cdm $^{-2}$
Image Lag		0.0001		-
Dark Test				
Dynamic Range		56.7		dB
VFPN Level		0.000265		Code/FSD
VFPN Max		0.000946		Code/FSD
HFPN Level		0.000643		Code/FSD
HFPN Max		0.000749		Code/FSD
Temporal Noise		-58.6		dB
Column Noise Level		-90.2		dB
Column Noise Max		-80.6		dB
Row Noise Level		-77.2		dB
Row Noise Max		-75.4		dB
Frame-to-Frame Flicker		0.000045		Codes
Dark Signal		-0.177105		Code/FSD.sec
Dark Signal Non-Uniformity		0.008845		Code/FSD.sec
PSRR @ 10kHz (2)				dB
PSRR @ 1MHz (2)				dB
PSRR @ 10MHz (2)				dB

[NOTE]
(1) Tested at Module-level (Except (1) and (2), other items are tested at Wafer-level.)
(2) Tested at analog_gain = 8x (max.) (Except (2), other items are tested at analog_gain = 1x.)

Table 6: AC Characteristics

(V_{DDH} = 2.8V, V_{DDL} = 1.8V ± 0.1V, T_A = -30 to + 70 °C, C_L = 10pF)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
Main input clock frequency	f_{MCLK}	Duty = 50%	6	13	27	MHz
Data output clock frequency	f_{PCLK}	-	4.05	32.5	65	
Propagation delay time from data output clock	t_{PDDV}	VSYNC output	-	-	TBD	
	t_{PDDH}	HSYNC output	-	-	TBD	
	t_{PDDO}	DATA output	-	-	TBD	
STBYN input pulse width	t_{WSHB}	STBYN=low(active)	TBD	-	-	

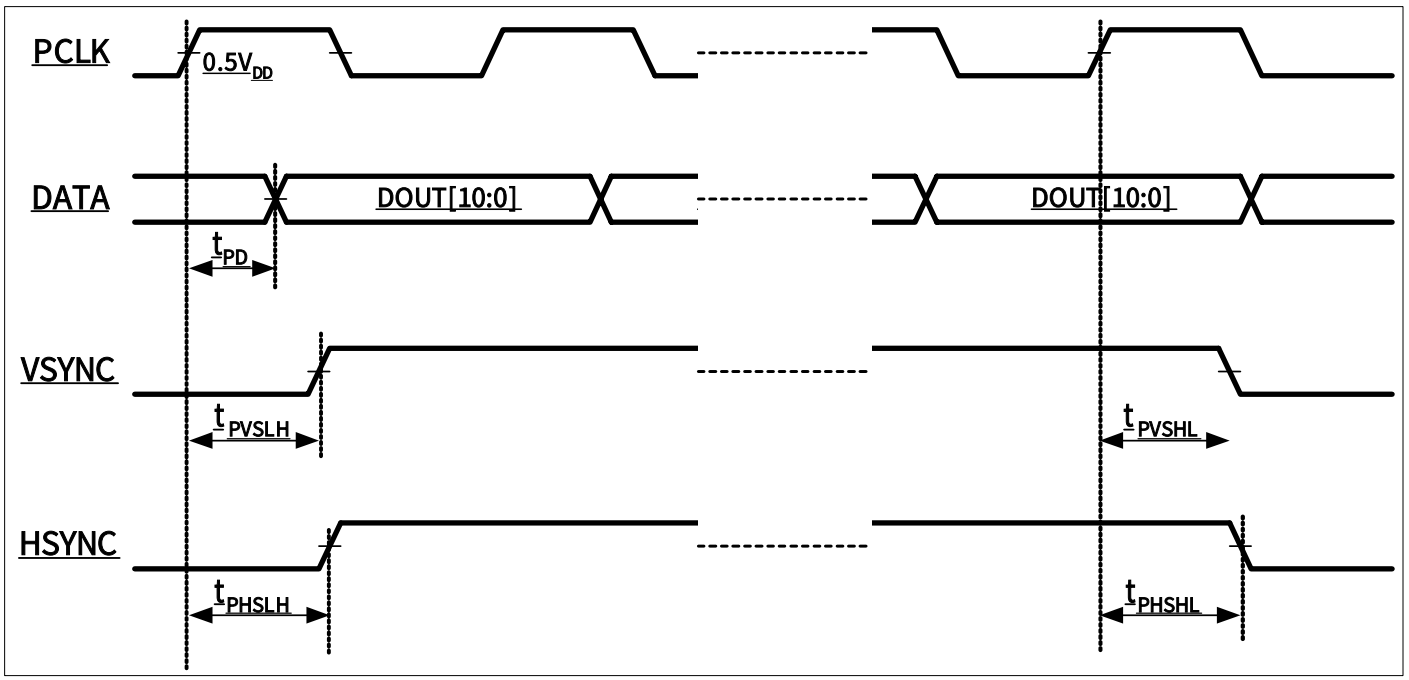


Figure 12: Propagation Delays for DCLK, Data Out, VSYNC, and HSYNC

Table 7: Electrostatic Characteristics

INDEX	Electrostatic Standard			UNIT	Remark
	PIN NO.	Design Target	Reference Product		
Human Body Model	ALL	TBD		V	
Machine Model	ALL	TBD		V	
CDM	I-test	±100mA		mA	
Latch-up	Power	Vdd max x 1.5		V	

REGISTER DESCRIPTION

Address	Default	Bits	Register name	Descriptions
00h	74h	[7:0]	chip_id	16-bit sensor model number (read-only), 0x7440
01h	40h	[7:0]		
02h	14h	[7]	pwr_save	Dynamic power save during VBLANK time
		[6]	mech_mod	Single frame capture integration mode with mechanical shutter
		[5]	htest_mod	Horizontal test mode 0b: disabled (default, pixel data displayed) 1b: enabled (black to white data displayed)
		[4]	shut_ctrl	Electronic shutter mode control 0b: shutter disabled, 1b: shutter enabled
		[3:2]	adc_res	ADC resolution selection 00b: 8-bit, 01b: 10-bit, 10b: 11-bit
		[1]	v_flip	Vertical flip control 0b: normal, 1b: vertical flip
		[0]	h_mirr	Horizontal mirror control 0b: normal, 1b: horizontal mirror
03h	00h	[4]	streaming	Active operation mode control 0b: stand-by, 1b: active operation mode
		[2]	pck_inv	PCK polarity inversion 0b: no inversion(default), 1b: inversion
		[1]	row_id_inv	(Reserved)
		[0]	sck_id_inv	(Reserved)
04h	00h	[4]	eds_test_mode	(Factory use only) Pixel accessibility control 0b: default access, 1b: extended access
		[3]	vs_inv	VSYNC polarity inversion 0b: active high, 1b: active low
		[2]	vs_disp	VSYNC display mode 0b: sync mode(default), 1b: data valid mode
		[1]	hs_inv	HSYNC polarity inversion 0b: active high, 1b: active low
		[0]	hs_disp	HSYNC display mode 0b: sync mode(default), 1b: data valid mode
06h	00h	[7:0]	vs_start	VSYNC start position
07h	00h	[7:0]		
08h	00h	[7:0]	vs_width	VSYNC width
09h	01h	[7:0]		
0Ah	00h	[7:0]	hs_start	HSYNC start position
0Bh	00h	[7:0]		
0Ch	00h	[7:0]	hs_width	HSYNC width
0Dh	20h	[7:0]		
10h	00h	[1]	gain_mode	Analog gain mode control 0b: global analog gain, 1b: per channel analog gain
		[0]	glb_gain_mode	Global gain mode control 0b : global sectional gain, 1b: per section gain
11h	00h	[7:0]	analogue_gain_code_global	Global analog gain control when gain_mode=0b
12h	00h	[7:0]	analogue_gain_code_greenR	Analog gain control for Gr

Address	Default	Bits	Register name	Descriptions
13h	00h	[7:0]	analogue_gain_code_red	Analog gain control for R
14h	00h	[7:0]	analogue_gain_code_blue	Analog gain control for B
15h	00h	[7:0]	analogue_gain_code_greenB	Analog gain control for Gb
16h	18h	[4:0]	global_gain_global	Global sectional gain control when glb_gain_mode=0b
17h	0Fh	[4:0]	global_gain_sec1	Global gain control for section 1
18h	0Fh	[4:0]	global_gain_sec2	Global gain control for section 2
19h	0Fh	[4:0]	global_gain_sec3	Global gain control for sectioin 3
1Ah	0Fh	[4:0]	global_gain_sec4	Global gain control for section 4
1Ch	09h	[7:0]	fine_integration_time[15:0]	Pixel integration time contorl in unit of pixel clock
1Dh	B8h	[7:0]		
1Eh	03h	[7:0]	coarse_integration_time[15:0]	Pixel integration time contorl in unit of line length
1Fh	67h	[7:0]		
20h	06h	[7:0]	frame_length_line[15:0]	Length of frame in unit of line length
21h	CEh	[7:0]		
22h	09h	[7:0]	line_length_dck[15:0]	Length of line in unit of data clock
23h	B8h	[7:0]		
24h	00h	[7:0]	x_addr_start[11:0]	X-address of the top left corner of the visible pixel data
25h	02h	[7:0]		
26h	00h	[7:0]	y_addr_start[11:0]	Y-address of the top left corner of the visible pixel data
27h	04h	[7:0]		
28h	08h	[7:0]	x_addr_end[11:0]	X-address of the bottom right corner of the visible pixel data
29h	09h	[7:0]		
2Ah	06h	[7:0]	y_addr_end[11:0]	Y-address of the bottom right corner of the visible pixel data
2Bh	0Bh	[7:0]		
2Ch	08h	[7:0]	x_output_size[11:0]	Width of image data output from the sensor
2Dh	10h	[7:0]		
2Eh	06h	[7:0]	y_output_size[11:0]	Height of image data output from the sensor
2Fh	10h	[7:0]		
30h	01h	[7:0]	x_even_inc[3:0]	Increment in x direction for even pixels - 0, 2, 4, etc.
31h	01h	[7:0]	x_odd_inc[3:0]	Increment in x direction for odd pixels - 1, 3, 5, etc.
32h	01h	[7:0]	y_even_inc[3:0]	Increment in y direction for even pixels - 0, 2, 4, etc.
33h	01h	[7:0]	y_odd_inc[3:0]	Increment in y direction for odd pixels - 1, 3, 5, etc.
40h	00h	[0]	offset_mode	(factory use only) Analog offset mode control 0b: global analog offset, 1b: per channel analog offset
41h	80h	[7:0]	offset_global	(factory use only) Global ananlog offset control when offset_mode=0b
42h	80h	[7:0]	offset_gr	(factory use only) Analog offset control for Gr
43h	80h	[7:0]	offset_r	(factory use only) Analog offset control for R
44h	80h	[7:0]	offset_b	(factory use only) Analog offset control for B

Address	Default	Bits	Register name	Descriptions
45h	80h	[7:0]	offset_gb	(factory use only) Analog offset control for Gb
46h	80h	[7:0]	offset_ref	(factory use only) Analog offset reference control
48h	29h	[5]	f_adlc_en	ADLC mode control
		[4]	ob_sel	(Reserved)
		[3:2]	gain_a	(Reserved)
		[1:0]	gain_b	(Reserved)
49h	00h	[7:0]	even_cnt_del	Digital offset control for Gr and Gb channels
4Ah	00h	[7:0]	odd_cnt_del	Digital offset control for R and B channels
4Ch	77h	[6:4]	(Reserved)	(Reserved)
		[2:0]	(Reserved)	(Reserved)
4Dh	FFh	[7:4]	(Reserved)	(Reserved)
		[3:0]	(Reserved)	(Reserved)
4Eh	F0h	[7:4]	(Reserved)	(Reserved)
		[3:0]	(Reserved)	(Reserved)
4Fh	F7h	[7:4]	(Reserved)	(Reserved)
		[2:0]	(Reserved)	(Reserved)
50h	04h	[7]	(Reserved)	(Reserved)
		[5:4]	(Reserved)	(Reserved)
		[3:0]	(Reserved)	(Reserved)
51h	88h	[7:0]	(Reserved)	(Reserved)
52h	05h	[6]	(Reserved)	(Reserved)
		[5]	(Reserved)	(Reserved)
		[4]	(Reserved)	(Reserved)
		[3:0]	(Reserved)	(Reserved)
53h	00h	[4]	(Reserved)	(Reserved)
		[0]	(Reserved)	(Reserved)
54h	04h	[4:0]	pll_p	Pre PLL clock divider control
56h	00h	[9:8]	pll_m	PLL multiplier control
57h	C8h	[7:0]		
58h	2h	[7:4]	dck_div1	Data clock divider 1 control
	Ah	[3:0]	dck_div2	Data clock divider 2 control
59h	2h	[7:4]	pck_div1	Pixel clock divider 1 control
	Ah	[3:0]	pck_div2	Pixel clock divider 2 control
60h	00h	[7:0]	scaling_mode	Scaling mode control
61h	10h	[7:0]	scale_m	Down scale factor control
62h	05h	[4:0]	(Reserved)	(Reserved)
63h	03h	[2:1]	clp_ctrl	(Reserved)
		[0]	clp_en_ctrl	Analog clamp control 0b: disabled, 1b: enabled
64h	06h	[7:0]	fifo_water_mark_pixels	(Reserved)
65h	10h	[7:0]		
66h	04h	[7:0]	(Reserved)	(Reserved)
67h	00h	[7]	ld_enable	(Reserved)

Address	Default	Bits	Register name	Descriptions
		[6:1]	(Reserved)	(Reserved)
		[0]	ave_sub_smp_en	(Reserved)
68h	08h	[3]	sda_en	(Reserved)
		[2]	sc1	(Reserved)
		[1]	sc0	(Reserved)
69h	01h	[7]	sync_mode	(Reserved)
		[6]	bpr_bit_sel	(Reserved)
		[5]	(Reserved)	(Reserved)
		[4]	out_hi_z	(Reserved)
		[3]	(Reserved)	(Reserved)
		[2]	(Reserved)	(Reserved)
		[1]	(Reserved)	(Reserved)
		[0]	dcen	(Reserved)
6Ah	A5h	[7:6]	YC_SC	(Reserved)
		[5:4]	DCLK_SC	(Reserved)
		[3:2]	SCL_SC	(Reserved)
		[1:0]	SDA_SC	(Reserved)
70h	33h	[7:4]	(Reserved)	(Reserved)
		[3:0]	(Reserved)	(Reserved)
71h	08h	[6]	(Reserved)	(Reserved)
		[5]	(Reserved)	(Reserved)
		[4]	(Reserved)	(Reserved)
		[3:0]	(Reserved)	(Reserved)
74h	00h	[3:2]	(Reserved)	(Reserved)
		[1:0]	(Reserved)	(Reserved)
75h	01h	[7:0]	(Reserved)	(Reserved)
80h	10h	[7]	(Reserved)	(Reserved)
		[6]	(Reserved)	(Reserved)
		[5]	(Reserved)	(Reserved)
		[4:0]	(Reserved)	(Reserved)
81h	10h	[7]	(Reserved)	(Reserved)
		[6]	(Reserved)	(Reserved)
		[5]	(Reserved)	(Reserved)
		[4:0]	(Reserved)	(Reserved)
82h	00h	[7:4]	(Reserved)	(Reserved)
		[1]	(Reserved)	(Reserved)
		[0]	(Reserved)	(Reserved)
83h	00h	[4:0]	(Reserved)	(Reserved)
84h	00h	[3:0]	(Reserved)	(Reserved)
90h	00h	[7:0]	(Reserved)	(Reserved)
91h	00h	[7:0]		(Reserved)
92h	00h	[7:0]	(Reserved)	(Reserved)
93h	00h	[7:0]		(Reserved)
94h	00h	[7:0]	(Reserved)	(Reserved)

Address	Default	Bits	Register name	Descriptions
95h	00h	[7:0]		(Reserved)
96h	00h	[7:0]	(Reserved)	(Reserved)
97h	00h	[7:0]		(Reserved)
98h	00h	[7:0]	(Reserved)	(Reserved)
99h	00h	[7:0]		(Reserved)
9Ah	00h	[7:0]	(Reserved)	(Reserved)
9Bh	00h	[7:0]		(Reserved)
9Ch	00h	[7:0]	(Reserved)	(Reserved)
9Dh	00h	[7:0]		(Reserved)
9Eh	00h	[7:0]	(Reserved)	(Reserved)
9Fh	00h	[7:0]		(Reserved)
A0h	00h	[7:0]	(Reserved)	(Reserved)
A1h	00h	[7:0]		(Reserved)
A2h	00h	[7:0]	(Reserved)	(Reserved)
A3h	00h	[7:0]		(Reserved)
A4h	00h	[7:0]	(Reserved)	(Reserved)
A5h	00h	[7:0]		(Reserved)
A6h	00h	[7:0]	(Reserved)	(Reserved)
A7h	00h	[7:0]		(Reserved)
A8h	00h	[7:0]	(Reserved)	(Reserved)
A9h	00h	[7:0]		(Reserved)
AAh	00h	[7:0]	(Reserved)	(Reserved)
ABh	00h	[7:0]		(Reserved)
ACh	00h	[7:0]	(Reserved)	(Reserved)
ADh	00h	[7:0]		(Reserved)
AEh	00h	[7:0]	(Reserved)	(Reserved)
AFh	00h	[7:0]		(Reserved)
B0h	00h	[7:0]	(Reserved)	(Reserved)
B1h	00h	[7:0]		(Reserved)
B2h	00h	[7:0]	(Reserved)	(Reserved)
B3h	00h	[7:0]		(Reserved)
B4h	00h	[7:0]	(Reserved)	(Reserved)
B5h	00h	[7:0]		(Reserved)
B6h	00h	[7:0]	(Reserved)	(Reserved)
B7h	00h	[7:0]		(Reserved)
B8h	00h	[7:0]	(Reserved)	(Reserved)
B9h	00h	[7:0]		(Reserved)
BAh	00h	[7:0]	(Reserved)	(Reserved)
BBh	00h	[7:0]		(Reserved)
BCh	00h	[7:0]	(Reserved)	(Reserved)
BDh	00h	[7:0]		(Reserved)
BEh	00h	[7:0]	(Reserved)	(Reserved)
BFh	00h	[7:0]		(Reserved)
C0h	00h	[7:0]	(Reserved)	(Reserved)

Address	Default	Bits	Register name	Descriptions
C1h	00h	[7:0]		(Reserved)
C2h	00h	[7:0]	(Reserved)	(Reserved)
C3h	00h	[7:0]		(Reserved)
C4h	00h	[7:0]	(Reserved)	(Reserved)
C5h	00h	[7:0]		(Reserved)
C6h	00h	[7:0]	(Reserved)	(Reserved)
C7h	00h	[7:0]		(Reserved)
C8h	00h	[7:0]	(Reserved)	(Reserved)
C9h	00h	[7:0]		(Reserved)
CAh	00h	[7:0]	(Reserved)	(Reserved)
CBh	00h	[7:0]		(Reserved)
CCh	00h	[7:0]	(Reserved)	(Reserved)
CDh	00h	[7:0]		(Reserved)
CEh	00h	[7:0]	(Reserved)	(Reserved)
CFh	00h	[7:0]		(Reserved)

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