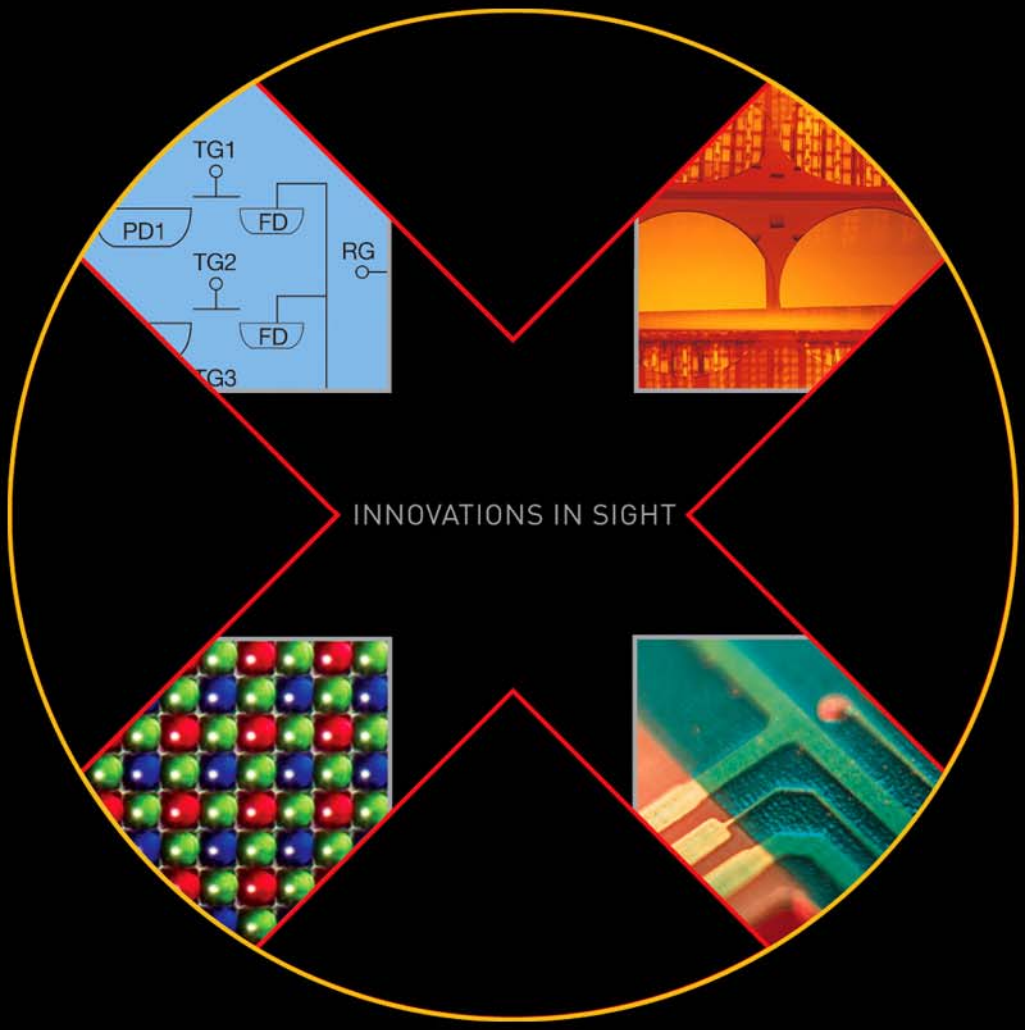
DEVICE PERFORMANCE SPECIFICATION

Revision 3.0 MTD/PS-0962

September 26, 2006



KODAK KAF-10500 IMAGE SENSOR

3970 (H) X 2646 (V) FULL-FRAME CCD COLOR IMAGE SENSOR

Kodak

Image Sensor Solutions

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TABLE OF CONTENTS

TABLE OF FIGURES

Kodak
Image Sensor Solutions

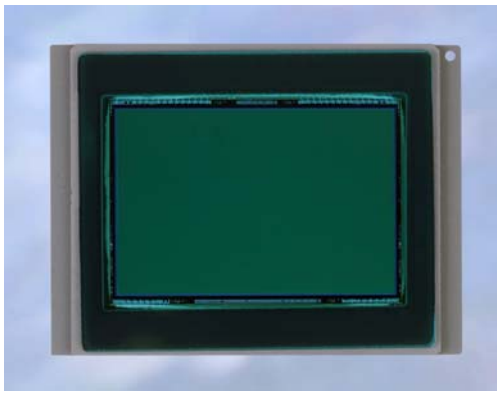
SUMMARY SPECIFICATION

KODAK KAF-10500 IMAGE SENSOR

3970 (H) X 2646 (V) FULL FRAME CCD COLOR IMAGE SENSOR

DESCRIPTION

The KAF-10500 is a dual output, high performance color CCD (charge coupled device) image sensor with 3970(H) x 2646(V) photoactive pixels designed for a wide range of color image sensing applications including digital imaging. Each pixel contains anti-blooming protection by means of a lateral overflow drain thereby preventing image corruption during high light level conditions. Each of the 6.8µm square pixels are selectively covered with red, green or blue pigmented filters for color separation. Microlenses are added for improved sensitivity. The total chip size is 28.7 mm x 20.2 mm and is housed in a 60 pin, 40.6 mm x 30.7 mm PGA ceramic package with 0.100" pin spacing.



FEATURES

- High resolution
- Broad dynamic range
- Low noise
- Large image area

APPLICATIONS

- Digital Still Cameras

Parameter	Typical Value
Architecture	Full Frame CCD (Square Pixels)
Total Number of Pixels	4098 (H) x 2728 (V) = 11.2 Mp
Number of Effective Pixels	4010 (H) x 2686 (V) = 10.8 Mp
Number of Active Pixels	3970 (H) x 2646 (V) = 10.5 Mp
Pixel Size	6.8 µm (H) x 6.8 µm (V)
Active Image Size	27.0 mm (H) x 18.0 mm (V) 32.44 mm (diagonal)
Aspect Ratio	3:2
Horizontal Outputs	2
Saturation Signal	60 ke^-
Output Sensitivity	25 $\mu V/e^-$
Quantum Efficiency (RGB)	21%, 40%, 32%
Read Noise (f=24 MHz)	15 e^-
Dark Signal (T=40 °C)	4 mV
Dark Current Doubling Temperature	6.3 °C
Linear Dynamic Range (f=24 MHz, T=40 °C)	71.5 dB
Charge Transfer Efficiency (HCTE/VCTE)	0.999995 0.999999
Blooming Protection (4 ms exposure time)	1000X saturation exposure
Maximum Data Rate	24 MHz
Package	Ceramic PGA
Cover Glass	IR Absorbing with AR Coating (both sides)

Parameters above specified at T = 20°C unless otherwise noted

ORDERING INFORMATION

Catalog Number	Product Name	Description	Marking Code
4H0799	KAF-10500-CXA-JH-AA-Offset	Color (Bayer RGB), Special Microlenses, PGA Package, IR Absorbing Cover Glass with AR coating (both sides), Standard grade	KAF-10500-CXA (Serial Number)
4H0800	KAF-10500-CXA-JH-AE-Offset	Color (Bayer RGB), Special Microlenses, PGA Package, IR Absorbing Cover Glass with AR coating (both sides), Engineering grade	
4H0846	KEK-4H0846-KAF-10500-12-24	Evaluation Board (Complete Kit)	N/A

Please see the User's Manual (MTD/PS-0982) for information on the Evaluation Kit for this part.

Please see ISS Application Note "Product Naming Convention" (MTD/PS-0892) for a full description of naming convention used for KODAK image sensors.

Address all inquiries and purchase orders to:

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DEVICE DESCRIPTION

ARCHITECTURE

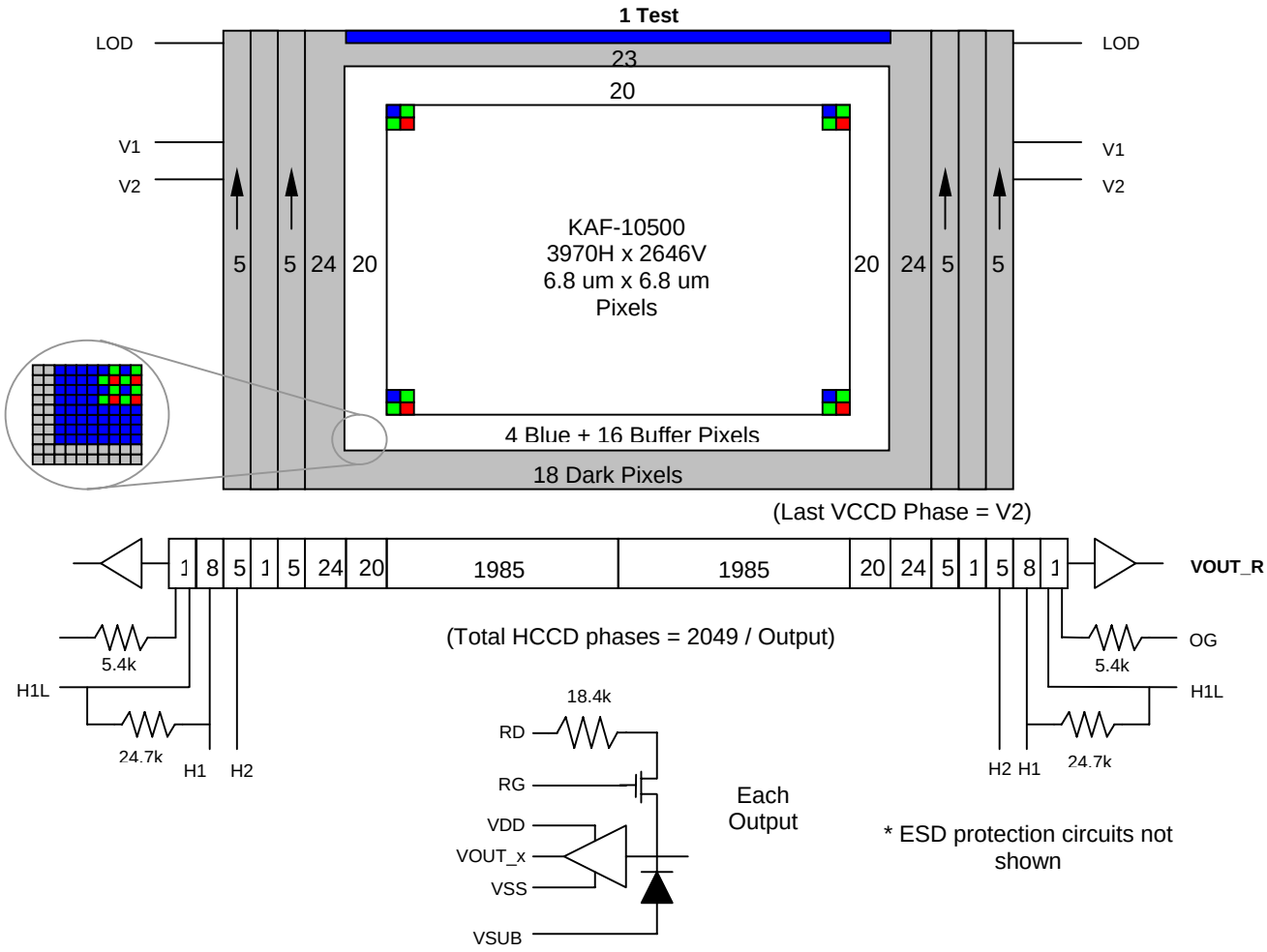


Figure 1: Block Diagram

Dark Reference Pixels

Surrounding the periphery of the device is a border of light shielded pixels creating a dark region. Within this dark region, exist light shielded pixels that include 24 leading dark pixels on every line. There are also 18 full dark lines at the start and 23 full dark lines at the end of every frame. Under normal circumstances, these pixels do not respond to light and may be used as a dark reference. Dummy Pixels.

Within each horizontal shift register there are 20 leading additional shift phases 1+8+5+1+5 (see Figure 1: Block Diagram). These pixels are designated as dummy pixels and should not be used to determine a dark reference level.

Active Buffer Pixels

There are 20 unshielded active buffer pixels between the photoactive area and the dark reference. These pixels are light sensitive but they are not tested for defects and non-uniformities. Of these 20 pixels, the outermost 4 pixels are covered with blue pigment while the remaining are arranged in a Bayer pattern (R, GR, GB, B)

IMAGE ACQUISITION

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the device. These photon-induced electrons are collected locally by the formation of potential wells at each photogate or pixel site. The number of electrons collected is linearly dependent on light level and exposure time and non-linearly dependent on wavelength. When the pixel's capacity is reached, excess electrons are discharged into the lateral overflow drain to prevent crosstalk or 'blooming'. During the integration period, the V1 and V2 register clocks are held at a constant (low) level.

CHARGE TRANSPORT

The integrated charge from each photogate (pixel) is transported to the output using a two-step process. Each line (row) of charge is first transported from the vertical CCD's to a horizontal CCD register using the V1 and V2 register clocks. The horizontal CCD is presented with a new line on the falling edge of V2 while H1 is held high. The horizontal CCD's then transport each line, pixel by pixel, to the output structure by alternately clocking the H1 and H2 pins in a complementary fashion. A separate connection to the last H1 phase (H1L) is provided to improve the transfer speed of charge to the floating diffusion output amplifier. On each falling edge of H1L a new charge packet is dumped onto a floating diffusion and sensed by the output amplifier.

HORIZONTAL REGISTER

Output Structure

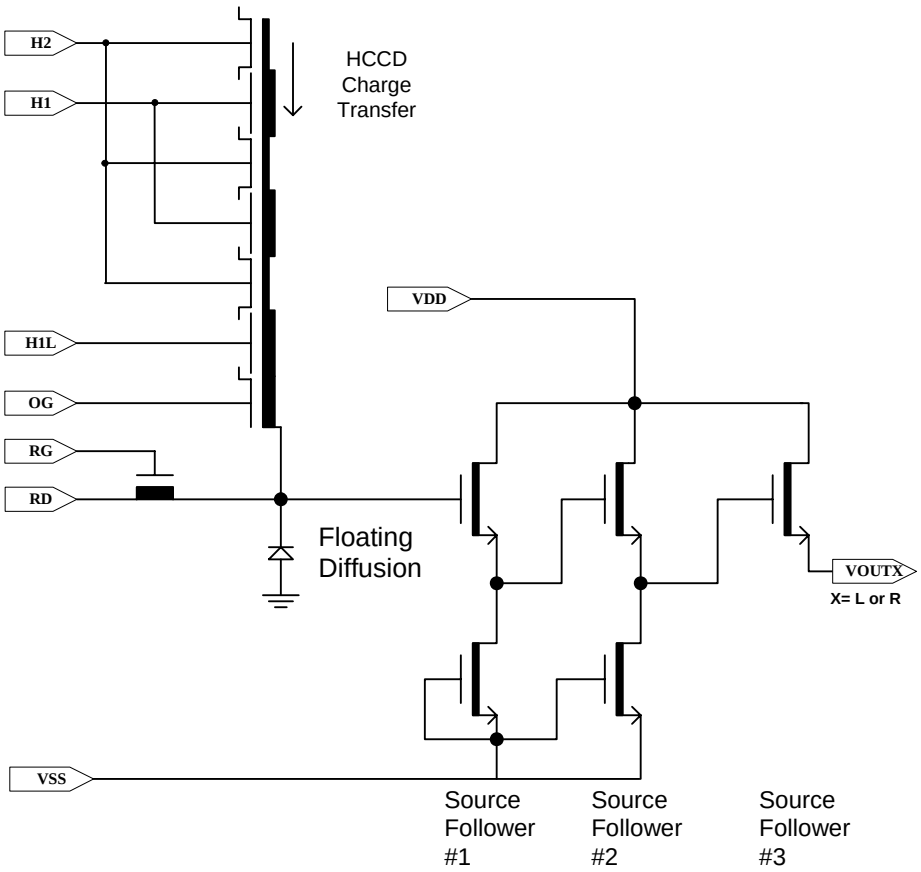


Figure 2: Output Architecture (Left or Right)

The output consists of a floating diffusion capacitance connected to a three-stage source follower. Charge presented to the floating diffusion (FD) is converted into a voltage and is current amplified in order to drive off-chip loads. The resulting voltage change seen at the output is linearly related to the amount of charge placed on the FD. Once the signal has been sampled by the system electronics, the reset gate (RG) is clocked to remove the signal and FD is reset to the potential applied by reset drain (RD). Increased signal at the floating diffusion reduces the voltage seen at the output pin. To activate the output structures, an off-chip current source must be added to the VOUT pins of the device. See Figure 3.

Output Load

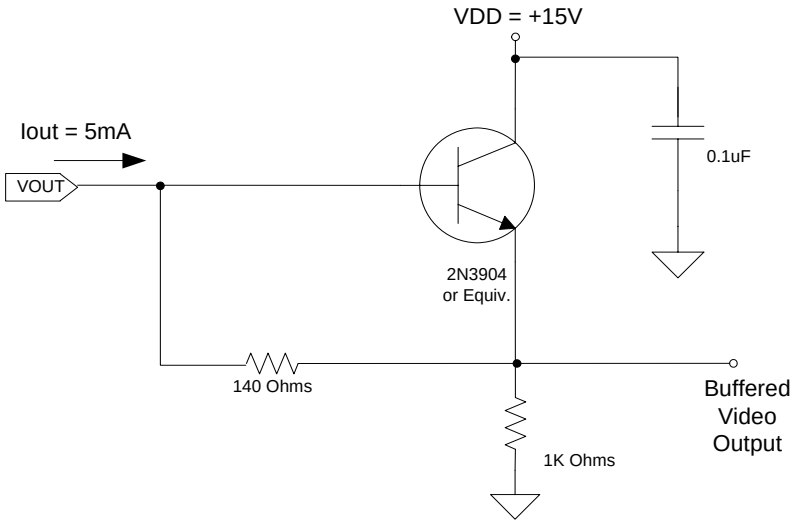
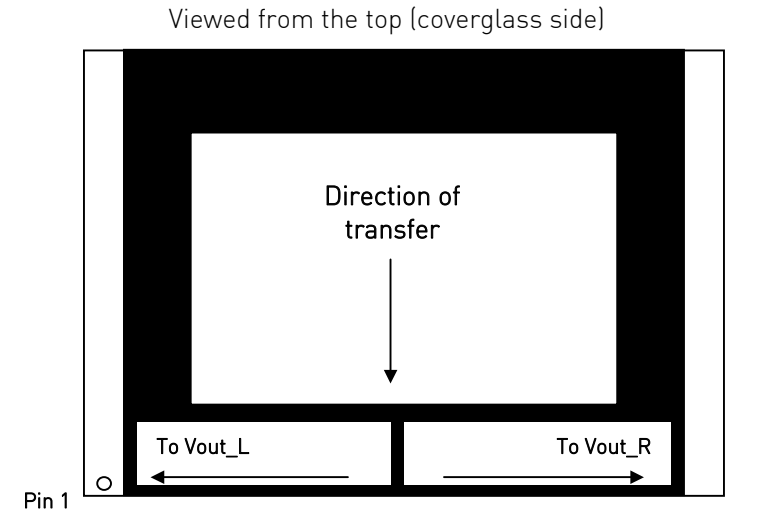


Figure 3: Typical Output Structure Load Diagram

Component values may be revised based on operating conditions and other design considerations

PHYSICAL DESCRIPTION

Pin Description and Device Orientation



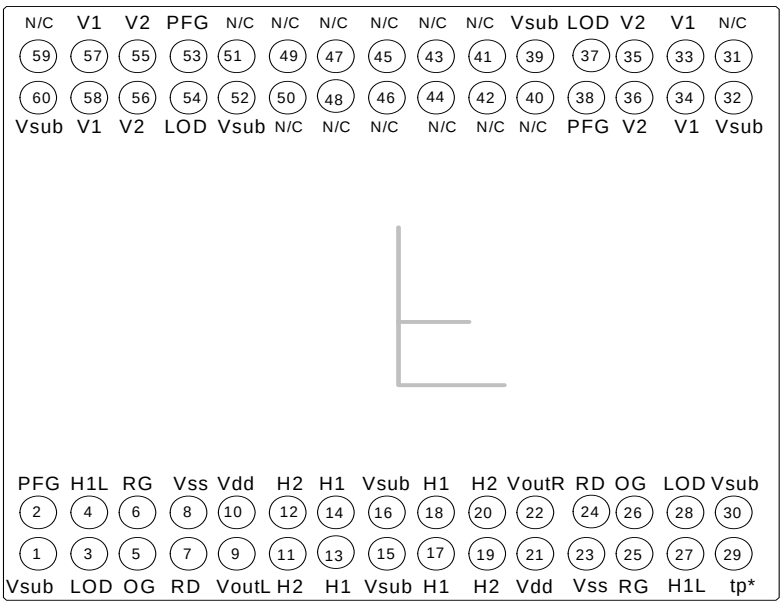


Figure 4: Pin out – Viewed from the top (coverglass side).

- Note: tp is a test point that is connected to Vsub internally. It should be left floating.

Pin	Name	Description
1	SUB	Substrate
2	PFG	No Connection
3	LOD	Lateral Overflow Drain
4	H1L	Horizontal Phase 1, Last Gate
5	OG	Output Gate
6	RG	Reset Gate
7	RD	Reset Drain
8	VSS	Output Amplifier Return
9	VOUTL	Video Output: Left
10	VDD	Output Amplifier Supply
11	H2	Horizontal Phase 2
12	H2	Horizontal Phase 2
13	H1	Horizontal Phase 1
14	H1	Horizontal Phase 1
15	SUB	Substrate
16	SUB	Substrate
17	H1	Substrate
18	H1	Horizontal Phase 1
19	H2	Horizontal Phase 1
20	H2	Horizontal Phase 2
21	VDD	Horizontal Phase 2
22	VOUTR	Output Amplifier Supply
23	VSS	Video Output:Right
24	RD	Output Amplifier Return
25	RG	Reset Drain
26	OG	Reset Gate
27	H1L	Output Gate
28	LOD	Horizontal Phase 1, Last Gate
29	tp*	Test point: leave unconnected or connect to Vsub
30	SUB	Substrate

Pin	Name	Description
60	SUB	Substrate
59	N/C	No Connection
58	V1	Vertical Phase 1
57	V1	Vertical Phase 1
56	V2	Vertical Phase 2
55	V2	Vertical Phase 2
54	LOD	Lateral Overflow Drain
53	PFG	No Connection
52	SUB	Substrate
51	N/C	No Connection
50	N/C	No Connection
49	N/C	No Connection
48	N/C	No Connection
47	N/C	No Connection
46	N/C	No Connection
45	N/C	No Connection
44	N/C	No Connection
43	N/C	No Connection
42	N/C	No Connection
41	N/C	No Connection
40	N/C	No Connection
39	SUB	Substrate
38	PFG	No Connection
37	LOD	Lateral Overflow Drain
36	V2	Vertical Phase 2
35	V2	Vertical Phase 2
34	V1	Vertical Phase 1
33	V1	Vertical Phase 1
32	SUB	Substrate
31	N/C	No Connection

Note: Pins with the same name are to be tied together on the circuit board and have the same timing.

*Note: tp is a test point that is connected to Vsub internally. It should be left floating or connected to Vsub.

IMAGING PERFORMANCE

TYPICAL OPERATIONAL CONDITIONS

Description	Condition - Unless otherwise noted	Notes
Frame time ($t_{readout}$ + t_{int})	572 ms	Includes overclock pixels
Integration time (tint)	250 ms	
Horizontal clock frequency	24 MHz	
Temperature	20 - 25 °C	Room temperature
Mode	integrate – readout cycle	
Operation	Nominal operating voltages and timing with min. vertical pulse width tVw = 15 µs	

SPECIFICATIONS

Description	Symbol	Min.	Nom.	Max	Units	Notes	Sample Plan
Saturation Signal	Vsat Ne^-_{sat} Q/V	1300 54k	1500 60k 25		mV e^- µV/e^-	1	die
Quantum Efficiency Red (630nm) Green (550nm) Blue (450 nm)	 Rr Rg Rb		 21 40 32		 % % %		 design design design
High Level Photoresponse Non-Linearity	PRNL			2	%	2	die
Photo Response Non-Uniformity	PRNU red PRNU g, b		12	3020	%p-p	3	die
Integration Dark Signal	Vdark,int		5	10	mV/s	4,16	die
Readout Dark Signal	Vdark,read		8	15	mV	15,16	die
Dark Signal Non-Uniformity	DSNU		1.5	4	mV p^- p	5	die
Dark Signal Doubling Temperature	DT		6.3		°C		design
Read Noise	NR		15	20	e^- rms		design
Total Noise	N		18	22	e^- rms	6	design
Linear Dynamic Range	DR		71.5		dB	7	design
Red-Green Hue Shift Blue-Green Hue Shift	RG Hue Unif BGHueUnif		4	10	%	8	die
Horizontal Charge Transfer Efficiency	HCTE		0.999995			9	die
Vertical Charge Transfer Efficiency	VCTE		0.999999				die
Blooming Protection	Xab	1000			x Vsat	10	design
DC Offset, output amplifier	Vodc	Vrd – 3.2	Vrd – 2.7	Vrd - 2	V	11	die
Output Amplifier Bandwidth	f.3dB	100	122	160	MHz	12	design
Output Impedance, Amplifier	ROUT	125	150	200	Ohms		die
Hclk Feedthru	Vhft		6	20	mV	13	die
Reset Feedthru	Vrft		1		V	14	design

Notes:

1. Increasing output load currents to improve bandwidth will decrease the conversion factor (Q/V).
2. Worst-case deviation (from 10 mV to Vsat min), relative to a linear fit applied between 0 and 85% of Vsatmin.
3. Difference between the maximum and minimum average signal levels of 146 x 146 blocks within the sensor on a per color basis as a % of average signal level.
4. T=60 °C. Average non-illuminated signal with respect to over-clocked vertical register signal.
5. T=60 °C. Absolute difference between the maximum and minimum average signal levels of 146 x 146 blocks within the sensor.
6. rms deviation of a multi-sampled pixel measured in the dark including amplifier and system noise sources.
7. 20log(Vsat/VN) - see Note 6 and note 1. VN = N_R * Q/V
8. Gradual variations in hue (red with respect to green pixels and blue with respect to green pixels) in regions of interest (146 x 146 blocks) within the sensor.
9. Measured per transfer at Vsat min. Typically, no degradation in CTE is observed up to 24 MHz.
10. Xab is the number of times above the Vsat illumination level that the sensor will bloom by spot size doubling. The spot size is 10% of the imager height. Xab is measured at 4ms.
11. Video level offset with respect to ground
12. Last stage only. Assumes 10 pF off-chip load.
13. Amount of artificial signal due to H1 coupling.
14. Amplitude of feedthrough pulse in VOUT due to RG coupling.
15. T=60 °C. Average non-illuminated signal collected due to the read out time.
16. Total dark signal = (Vdark,int x tint)+ Vdark,read

TYPICAL PERFORMANCE CURVES

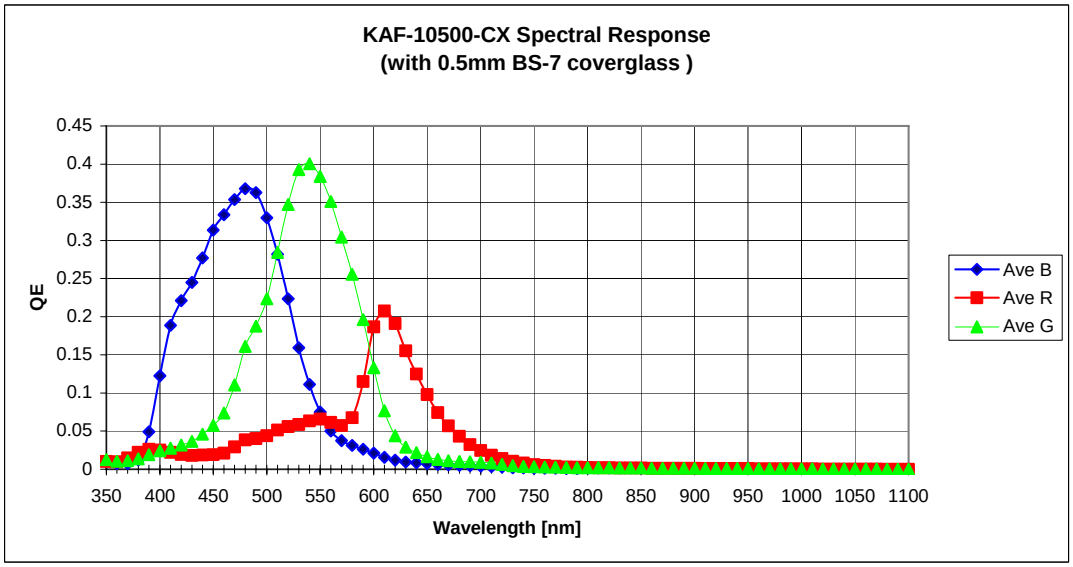


Figure 5: Typical Spectral Response with coverglass

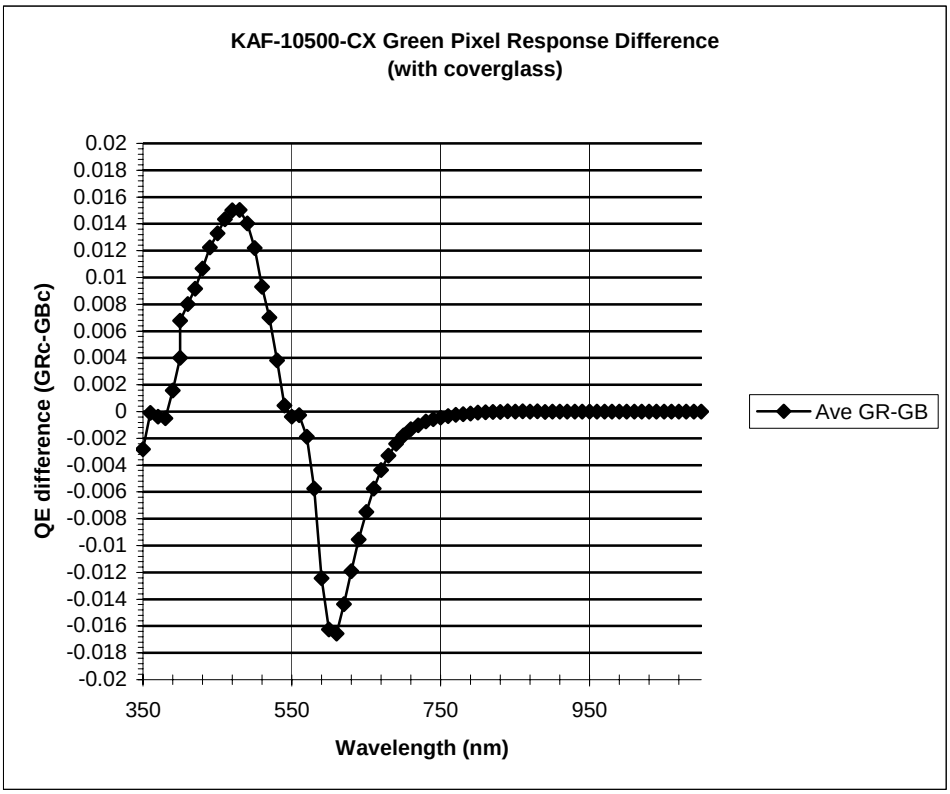


Figure 6: Typical Green (Red row)–Green (Blue row) QE Difference with coverglass

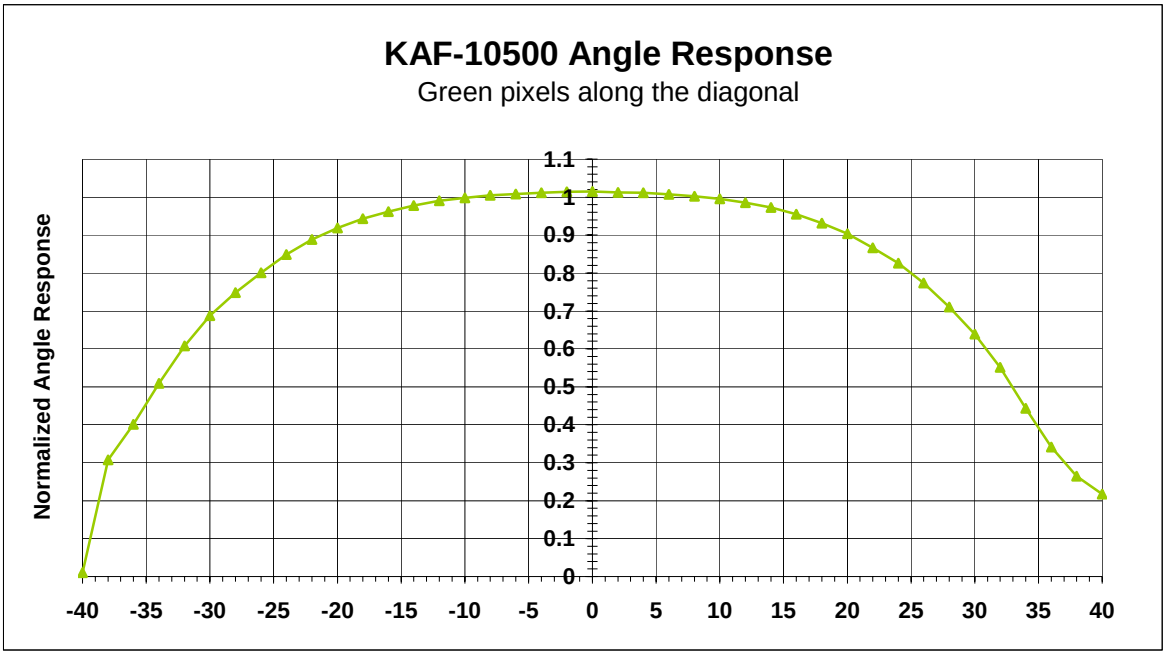


Figure 7: Typical Angle QE Response

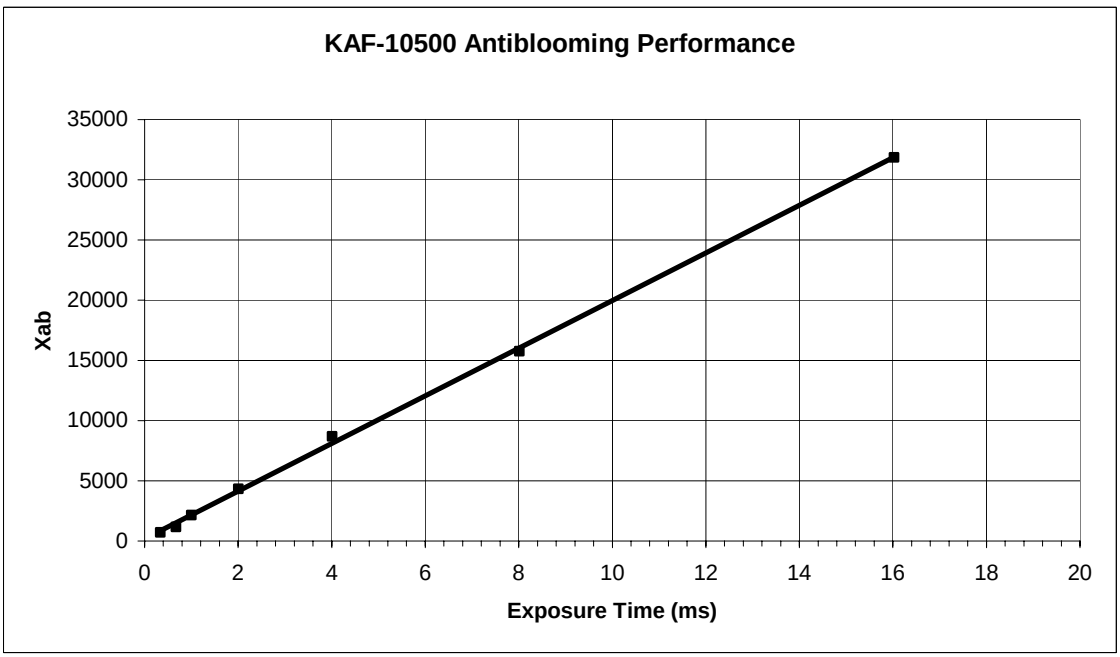


Figure 8: Typical Antiblooming Performance

DEFECT DEFINITIONS

OPERATING CONDITIONS

All defect tests performed at T>20 °C, t_{int} = 250 ms and $t_{readout}$ = 322 ms

SPECIFICATIONS

Classification	Points	Clusters	Columns	Includes dead columns
Standard Grade	<2,500	<30	<10	yes

Point Defects

A pixel that deviates by more than 9 mV above neighboring pixels under non-illuminated conditions

-- OR --

A pixel that deviates by more than 7% above or 11% below neighboring pixels under illuminated conditions

Cluster Defect

A grouping of not more than 10 adjacent point defects Cluster defects are separated by no less than 4 good pixels in any direction

Column Defect

A grouping of more than 10 point defects along a single column

-- OR --

A column that deviates by more than 0.9 mV above or below neighboring columns under non-illuminated conditions

-- OR --

A column that deviates by more than 1.5% above or below neighboring columns under illuminated conditions

Column and cluster defects are separated by at least 4 good columns in the x direction. No multiple column defects (double or more) will be permitted.

Dead Columns

A column that deviates by more than 50% below neighboring columns under illuminated conditions

Saturated Columns

A column that deviates by more than 100mV above neighboring columns under non-illuminated conditions. No saturated columns are allowed

OPERATION

ABSOLUTE MAXIMUM RATINGS

Description	Symbol	Minimum	Maximum	Units	Notes
Diode Pin Voltages	Vdiode	-0.5	+17.5	V	1,2
Gate Pin Voltages	Vgate1	-13.5	+13.5	V	1,3
Gate - Gate Voltages	V1-2	-13.5	+13.5	V	4,5
Output Bias Current	Iout		-30	mA	6
LOD Diode Voltage	VLODT	-0.5	+13.0	V	7
Operating Temperature	TOP	0	60	°C	8

Notes:

1. Referenced to pin SUB
2. Includes pins: RD, VDD, VSS, VOUT.
3. Includes pins: V1, V2, H1, H1L, H2, RG, OG.
4. Voltage difference between overlapping gates. Includes: V1 to V2; H1, H1L to H2; H1L to OG; V1 to H2. These inputs contain an ESD protection circuit. Exceeding the maximum voltages will cause an uncontrolled current to flow in these circuits and may damage the input pin.
5. Voltage difference between non-overlapping gates. Includes: V1 to H1, H1L; V2, OG to H2. These inputs contain an ESD protection circuit. Exceeding the maximum voltages will cause an uncontrolled current to flow in these circuits and may damage the input pin.
6. Avoid shorting output pins to ground or any low impedance source during operation. Amplifier bandwidth increases at higher currents and lower load capacitance at the expense of reduced gain (sensitivity). Operation at the maximum values will reduce Mean Time to Failure (MTTF).
7. V1, H1, V2, H2, H1L, OG, and RD are tied to 0 V.
8. Noise performance will degrade at higher temperatures.
9. Absolute maximum rating is defined as a level or condition that should not be exceeded at any time per the description. If the level or condition is exceeded, the device will be degraded and may be damaged.

POWER-UP SEQUENCE

The sequence chosen to perform an initial power-up is not critical for device reliability. A coordinated sequence may minimize noise and the following sequence is recommended:

a. Connect the ground pins (SUB).
b. Supply the appropriate biases and clocks to the remaining pins.

DC BIAS OPERATING CONDITIONS

Description	Symbol	Minimum	Nominal	Maximum	Units	Maximum DC Current (mA)	Notes
Reset Drain	RD	11.3	11.5	11.7	V	IRD = 0.01	
Output Amplifier Return	VSS	0.5	0.7	1.0	V	ISS = 3.0	
Output Amplifier Supply	VDD	14.5	15.0	15.5	V	IOUT + ISS	
Substrate	SUB		0		V	0.01	
Output Gate	OG	-3.2	-3.0	-2.8	V	0.01	
Lateral Drain	LOD	9.8	10.0	10.2	V	0.01	
Video Output Current	IOUT		-5	-10	mA		1

Note:

1. An output load sink must be applied to VOUT to activate output amplifier - see Figure 3.

AC OPERATING CONDITIONS

Clock Levels

Description	Symbol	Level	Minimum	Nominal	Maximum	Units	Effective Capacitance	Notes
V1 Low Level	V1L	Low	-9.2	-9.0	-8.8	V	150 nF	1,2
V1 High Level	V1H	High	2.3	2.5	2.7	V		1
V2 Low Level	V2L	Low	-9.2	-9.0	-8.8	V	280 nF	1,2
V2 High Level	V2H	High	2.3	2.5	2.7	V		1
H1 Low Level	H1L	Low	-4.7	-4.5	-4.3	V	309 pF	1
H1 High Level	H1H	High	2.5	2.7	2.9	V		1
H1L Low Level	H1Llow,	Low	-6.7	-6.5	-6.3	V	8 pF	1, 2
H1L High Level	H1Lhigh	High	2.5	2.7	2.9	V		1
H2 Low Level	H2L	Low	-5.2	-5.0	-4.8	V	208 pF	1, 2
H2 High Level	H2H	High	2.0	2.2	2.4	V		1
RG Low Level	RGL	Low	0.3	0.5	0.7	V	8 pF	1, 2
RG High Level	RGH	High	7.8	8.0	8.2	V		1

Notes:

1. All pins draw less than 10 mA DC current. Capacitance values relative to SUB (substrate).
2. Clock capacitance is the effective capacitance extrapolated from the rise and fall time measured while operating the sensor.

TIMING

REQUIREMENTS AND CHARECTERISTICS

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
H1, H2 Clock Frequency	fH			24	MHz	1, 2
V1, V2 Clock Frequency	fV			83.3	kHz	1, 2
H1, H2 Rise, Fall Times	t H1r , t H1f	5		10	%	3, 7
V1, V2 Rise, Fall Times	t V1r , t V1f	5		10	%	3
V1 - V2 Cross-over	V VCR	-1	0	1	V	
H1 - H2 Cross-over	V HCR	-2.8	-1.4	0	V	
H1L Rise – H2 Fall Crossover	V H1LCR	-2.0		1.0	V	9
H1, H2 Setup Time	tHS	1	5		µs	
RG Clock Pulse Width	tRGw	5			ns	4
RG Rise, Fall Times	t RGr , t RGf	5		10	%	3
V1, V2 Clock Pulse Width	tVw	6			µs	2, 6
Flush clock off time	toff	4			µs	2, 6
Pixel Period (1 Count)	t_e	42			ns	
H1L – VOUT Delay	t_{HV}		5		ns	
RG - VOUT Delay	t_{RV}		5		ns	
Readout Time	$t_{readout}$	268			ms	6, 8
Integration Time	t_{int}		-			5, 6
Line Time	t_{line}	98.4			µs	6
Fast Flush Time	t_{flush}	40			ms	

Notes:

1. 50% duty cycle values.
2. CTE will degrade above the nominal frequency.
3. Relative to the pulse width (based on 50% of high/low levels).
4. RG should be clocked continuously.
5. Integration time is user specified.
6. Longer times will degrade noise performance.
7. The maximum specification or 10nsec whichever is greater based on the frequency of the horizontal clocks.
8. $t_{readout} = t_{line} * 2728$ lines.
9. The charge capacity near the output could be degraded if the voltage at the clock cross over point is outside this range.

EDGE ALIGNMENT

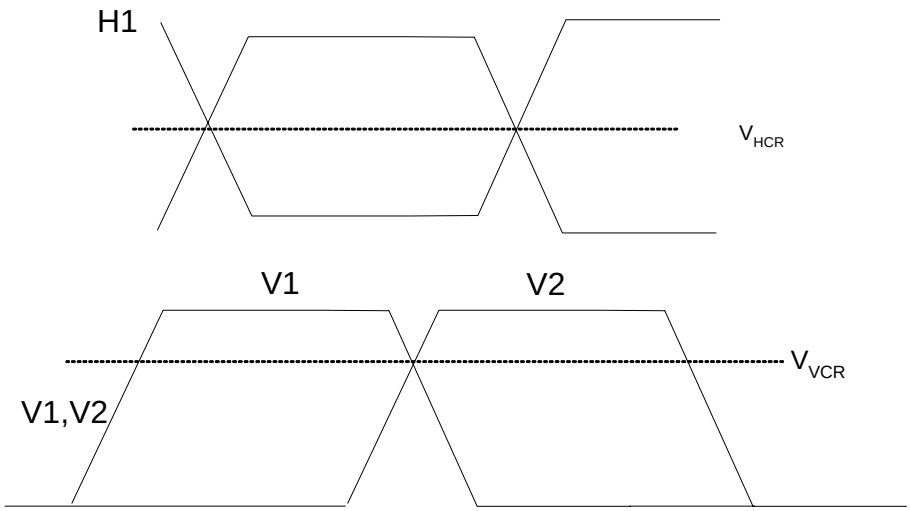


Figure 9: Timing Edge Alignment

FRAME TIMING

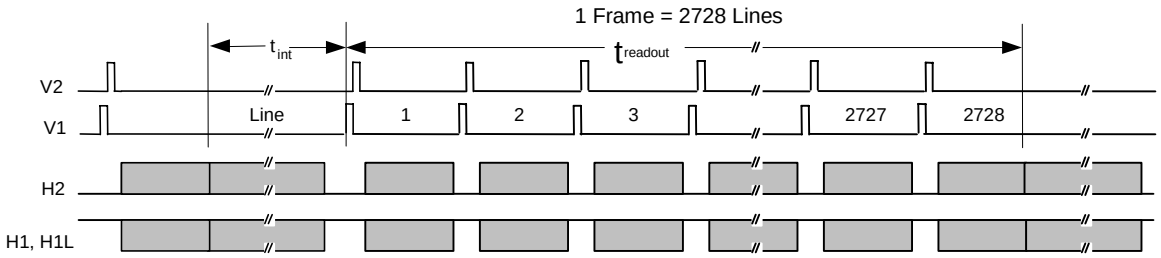


Figure 10: Frame Timing

Frame Timing Detail

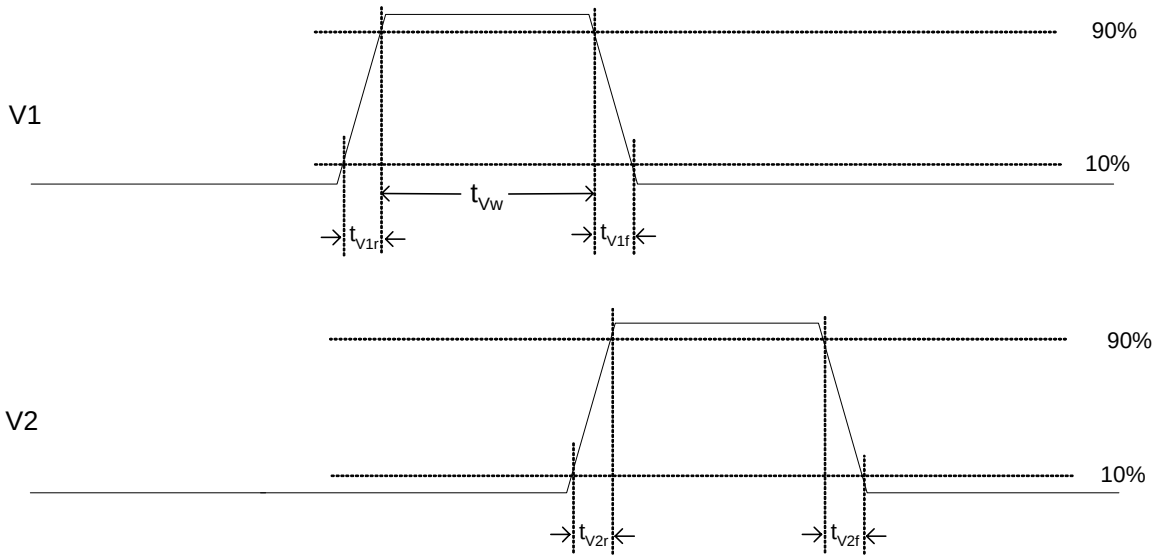


Figure 11: Frame Timing Detail

LINE TIMING (EACH OUTPUT)

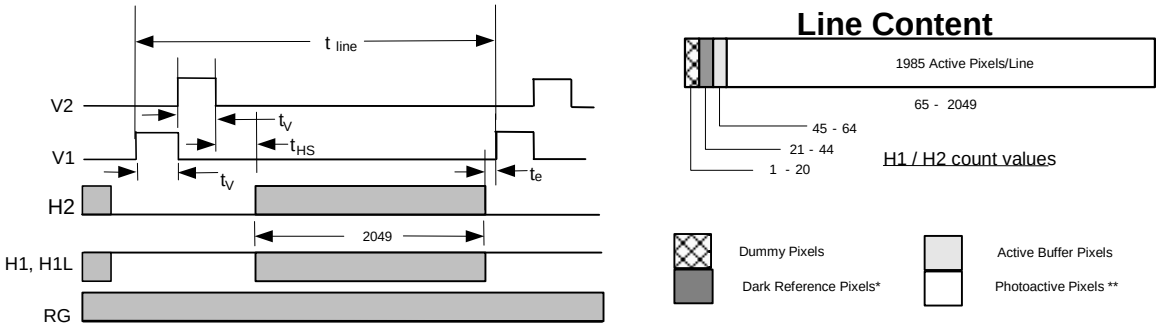


Figure 12: Line Timing

PIXEL TIMING

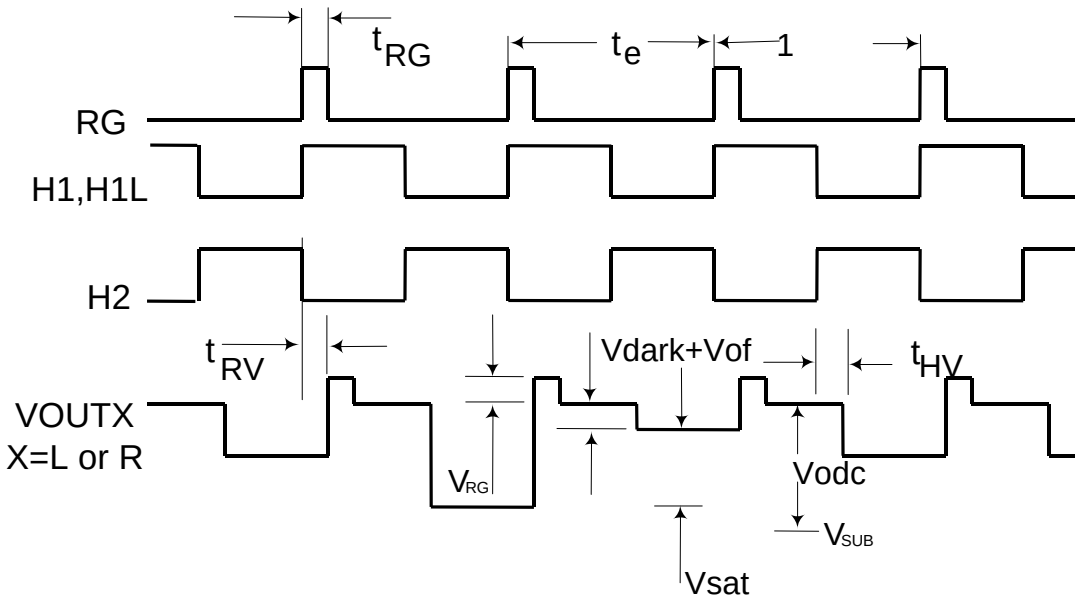


Figure 13: Pixel Timing

Pixel Timing Detail

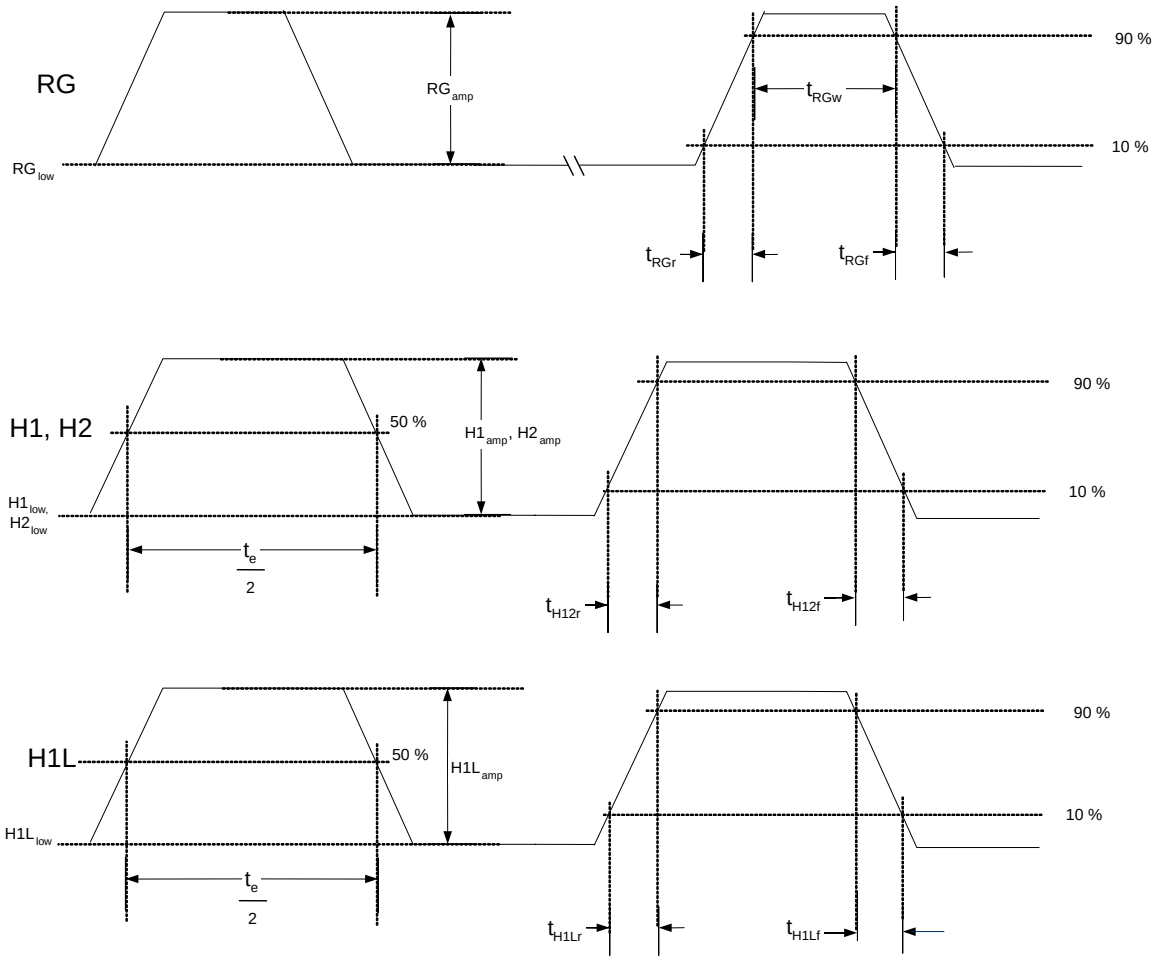


Figure 14: Pixel Timing Detail

MODE OF OPERATION

POWER-UP-FLUSH CYCLE

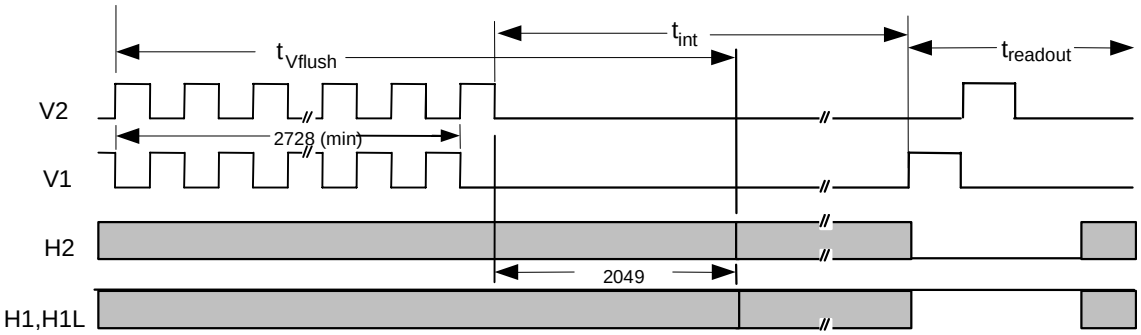


Figure 15: Power-up Flush Cycle

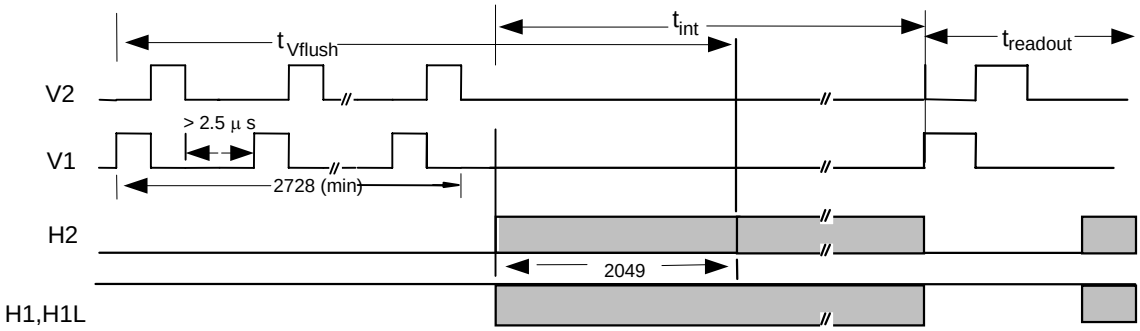


Figure 16: Modified (Slow) Flush Cycle

STORAGE AND HANDLING

STORAGE CONDITIONS

Description	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	TST	-20	70	°C	1

Notes:
1. Long-term storage toward the maximum temperature will accelerate color filter degradation.
2. T=25° C. Excessive humidity will degrade MTTF.

ESD

1. This device contains limited protection against Electrostatic Discharge (ESD). CCD image sensors can be damaged by electrostatic discharge. Failure to do so may alter device performance and reliability.
2. Devices should be handled in accordance with strict ESD procedures for Class 0 (<250V per JESD22 Human Body Model test), or Class A (<200V JESD22 Machine Model test) devices. Devices are shipped in static-safe containers and should only be handled at static-safe workstations.
3. See Application Note MTD/PS-0224 "Electrostatic Discharge Control for Image Sensors" for proper handling and grounding procedures. This application note also contains recommendations for workplace modifications for the minimization of electrostatic discharge.
4. Store devices in containers made of electro-conductive materials.

COVER GLASS CARE AND CLEANLINESS

1. The cover glass is highly susceptible to particles and other contamination. Perform all assembly operations in a clean environment.
2. Touching the cover glass must be avoided.
3. Improper cleaning of the cover glass may damage these devices. Refer to Application Note MTD/PS-0237 "Cover Glass Cleaning for Image Sensors".

ENVIRONMENTAL EXPOSURE

1. Do not expose to strong sun light for long periods of time. The color filters and/or microlenses may become discolored. Long time exposures to a static high contrast scene should be avoided. The image sensor may become discolored and localized changes in response may occur from color filter/microlens aging.
2. Exposure to temperatures exceeding the absolute maximum levels should be avoided for storage and operation. Failure to do so may alter device performance and reliability.
3. Avoid sudden temperature changes.
4. Exposure to excessive humidity will affect device characteristics and should be avoided. Failure to do so may alter device performance and reliability.
5. Avoid storage of the product in the presence of dust or corrosive agents or gases.

Long-term storage should be avoided. Deterioration of lead solderability may occur. It is advised that the solderability of the device leads be re-inspected after an extended period of storage, over one year.

SOLDERING RECOMMENDATIONS

1. The soldering iron tip temperature is not to exceed 370°C. Failure to do so may alter device performance and reliability.
2. Flow soldering method is not recommended. Solder dipping can cause damage to the glass and harm the imaging capability of the device. Recommended method is by partial heating. Kodak recommends the use of a grounded 30W soldering iron. Heat each pin for less than 2 seconds duration.

MECHANICAL INFORMATION

COMPLETED ASSEMBLY

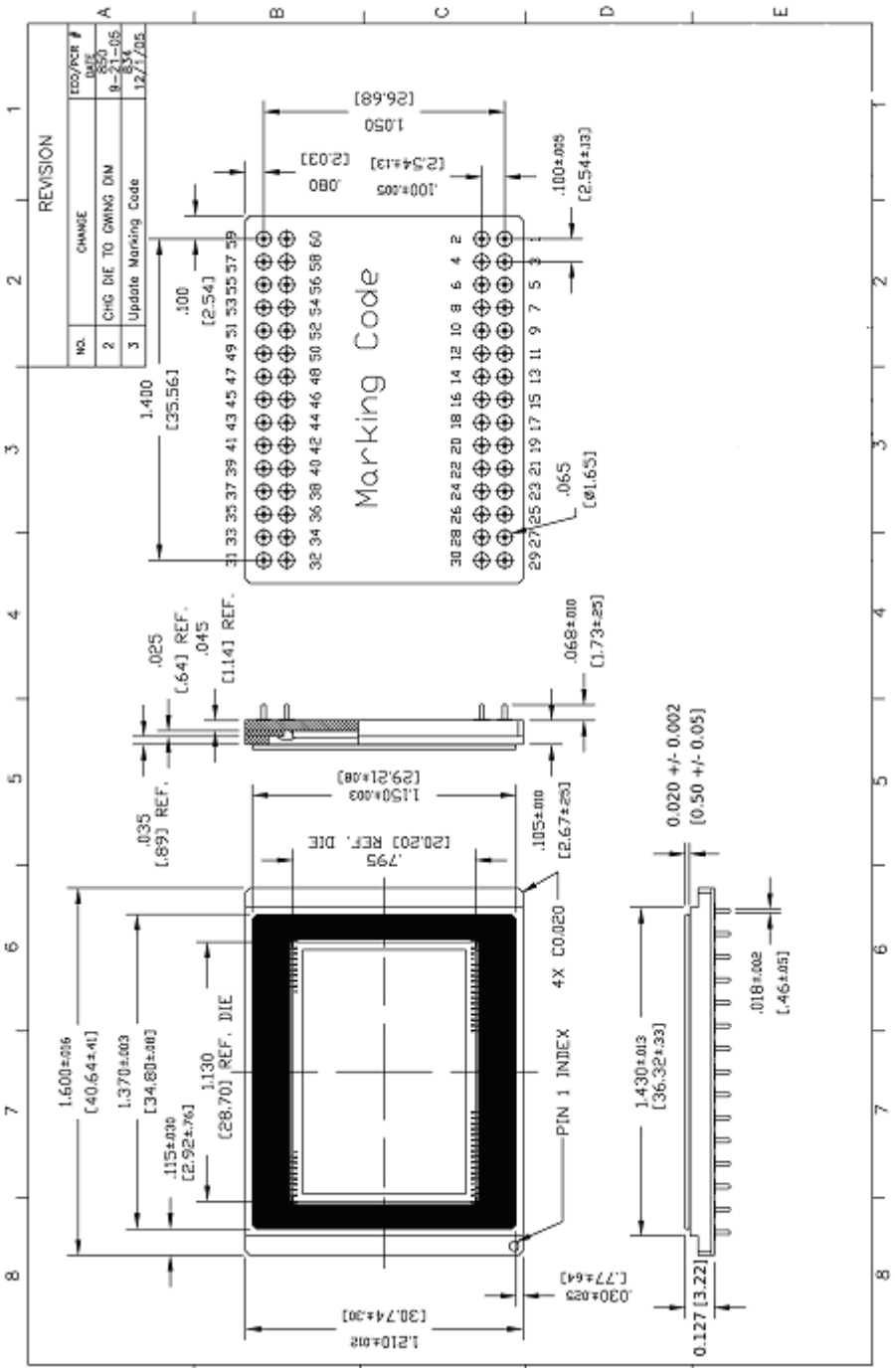


Figure 17: Completed Assembly (1 of 2)

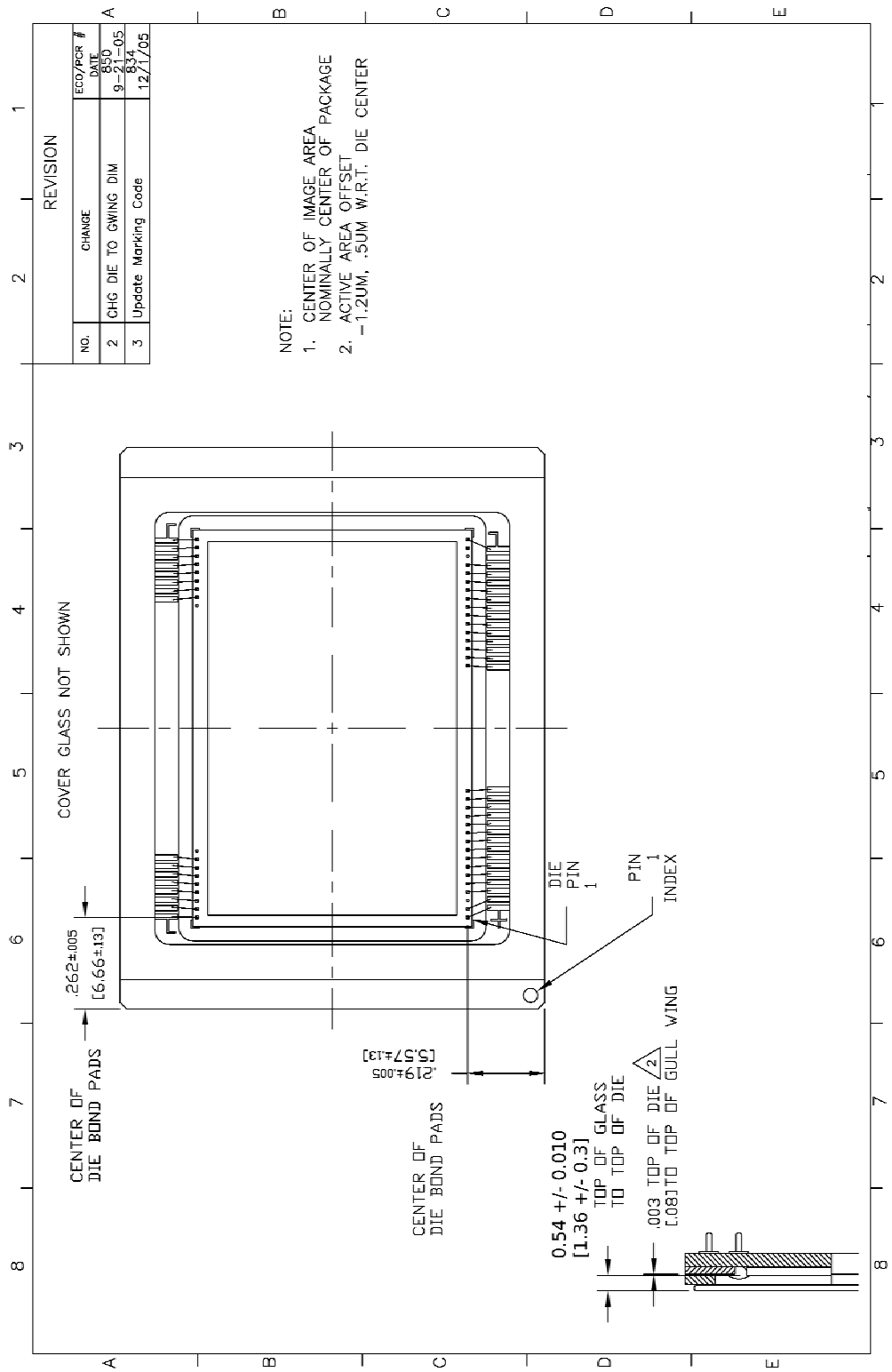


Figure 18: Completed Assembly (2 of 2)

COVER GLASS SPECIFICATION

1. Scratch and dig: 20 micron max
2. Substrate material: Kyocera B-7
3. Multilayer anti-reflective coating

Wavelength	Transmission
400 nm	> 80%
420 – 530 nm	> 90%
610 – 630 nm	50% crossover point
710 – 750 nm	< 10%
750 – 1000 nm	< 5%
1000 – 1100 nm	< 10%

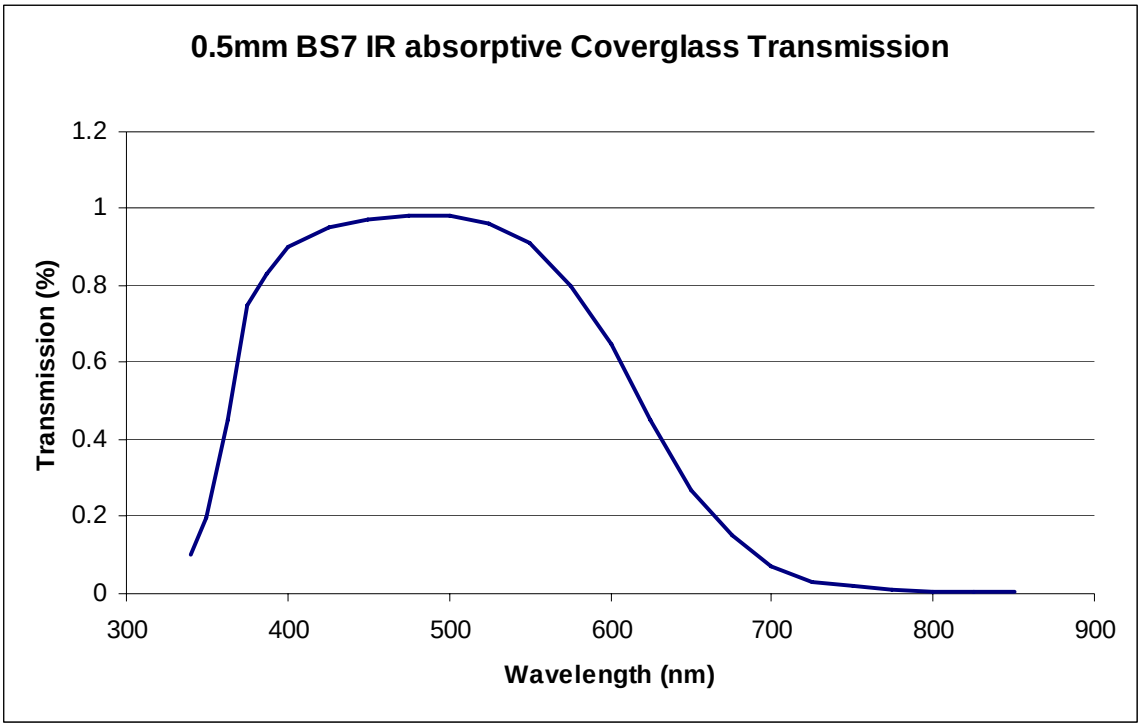


Figure 19: Cover Glass Transmission

QUALITY ASSURANCE AND RELIABILITY

QUALITY STRATEGY

All image sensors will conform to the specifications stated in this document. This will be accomplished through a combination of statistical process control and inspection at key points of the production process. Typical specification limits are not guaranteed but provided as a design target. For further information refer to ISS Application Note MTD/PS-0292, Quality and Reliability.

REPLACEMENT

All devices are warranted against failure in accordance with the terms of Terms of Sale. This does not include failure due to mechanical and electrical causes defined as the liability of the customer below.

LIABILITY OF THE SUPPLIER

A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer.

LIABILITY OF THE CUSTOMER

Damage from mechanical (scratches or breakage), electrostatic discharge (ESD) damage, or other electrical misuse of the device beyond the stated absolute maximum ratings, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.

RELIABILITY

Information concerning the quality assurance and reliability testing procedures and results are available from the Image Sensor Solutions and can be supplied upon request. For further information refer to ISS Application Note MTD/PS-0292, Quality and Reliability.

TEST DATA RETENTION

Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.

MECHANICAL

The device assembly drawing is provided as a reference. The device will conform to the published package tolerances.

Kodak reserves the right to change any information contained herein without notice. All information furnished by Kodak is believed to be accurate.

WARNING: LIFE SUPPORT APPLICATIONS POLICY

Kodak image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of the Eastman Kodak Company. Product warranty is limited to replacement of defective components and does not cover injury or property or other consequential damages.

REVISION CHANGES

Revision Number	Description of Changes
1.0	Initial Release.
2.0	Changed ms to µs. Changed MV to mV.
3.0	Timing- Changed Readout time and Fast Flush time from µs to ms.

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