DATA SHEET

FTF2416C

4M Full-Frame CCD Image Sensor

Preliminary specification

2003 February 6

DALSA
Professional Imaging

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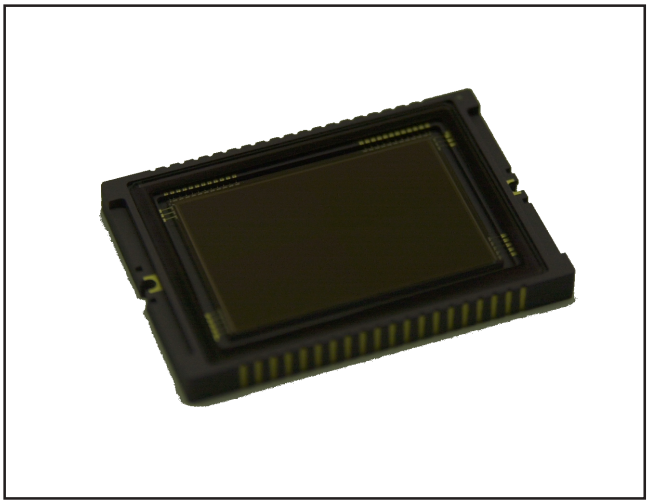
4M Full-Frame CCD Image Sensor FTF2416C

- **APS compatible optical image format**
- **4M active pixels (2460H x 1640V)**
- **RGB Bayer pattern**
- **Progressive scan**
- **Excellent anti-blooming**
- **Variable electronic shuttering**
- **Vertical subsampling**
- **Square pixel structure**
- **H and V binning**
- **90% optical fill factor**
- **High linear dynamic range (>72dB)**
- **High sensitivity**
- **Low dark current and fixed-pattern noise**
- **Low read-out noise**
- **Data rate up to 27 MHz**
- **Mirrored and split read-out**
- **Perfectly matched to visual spectrum**



Description

The FTF2416C is a full frame CCD colour image sensor designed for professional digital photography applications, with very low dark current and a linear dynamic range of over 12 true bits at room temperature. The two low-noise output amplifiers, one at each corner of the output register, make the FTF2416C suitable for a wide range of high-end visual light applications. With one output amplifier, a progressively scanned image can be read out at 5 frames per second. By using multiple outputs the frame rate increases accordingly. The device structure is shown in figure 1.

Device structure

Optical size:	22.140 mm (H) x 14.760 mm (V)	
Chip size:	23.900 mm (H) x 16.000 mm (V)	
Pixel size:	9 µm x 9 µm	
Active pixels:	2460 (H) x 1640 (V)	
Total no. of pixels:	2508 (H) x 1652 (V)	
Optical black pixels:	Left: 20	Right: 20
Timing pixels:	Left: 4	Right: 4
Dummy register cells:	Left: 7	Right: 7
Optical black lines:	Bottom: 6	Top: 6

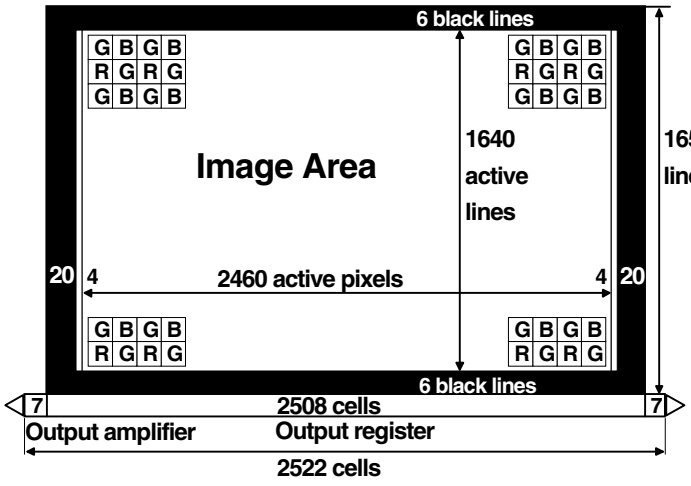


Figure 1 - Device structure

Architecture of the FTF2416C

The optical centers of all pixels in the image section are aligned on a square grid. The charge is generated and integrated in this section. An output register is located below the image section for read-out. After the integration time, the image charge is shifted one line at the time to the register. A separate transfer gate (TG) between the image section and output register will enable sub-sampling features. The left and the right half of the register can be controlled independently. This enables either single or multiple read-out. The register can be used for vertical binning. A summing gate at both ends of the register can be used for horizontal binning (see figure 2).

IMAGE SECTION	
Image diagonal (active video only)	27.97 mm
Aspect ratio	3:2
Active image width x height	22.140 x 14.760 mm^2
Pixel width x height	9 x 9 μm^2
Geometric fill factor	90%
Image clock pins	8 pins (A1..A4), left and right connected in sensor
Capacity of each clock phase	2.0 nF per pin
Number of active lines	1640
Number of black reference lines	4 (=2x2)
Number of dummy black lines	8 (=2x4)
Total number of lines	1652
Number of active pixels per line	2460
Number of overscan (timing) pixels per line	8 (2x4)
Number of black reference pixels per line	40 (2x20)
Total number of pixels per line	2508

OUTPUT REGISTER	
Output buffers	2 x Three-stage source followers
Number of dummy cells per register	14 (2x7)
Number of register cells per register	2522 (2508+14)
Output register horizontal transport clock pins	6 pins per register (C1..C3), left and right
Capacity of each C-clock phase	100 pF per pin
Overlap capacity between neighbouring C-clocks	25 pF
Output register Summing Gates	2 pins (SG)
Capacity of each SG	15 pF
Reset Gate clock phases	2 pins (RG)
Capacity of each RG	15 pF

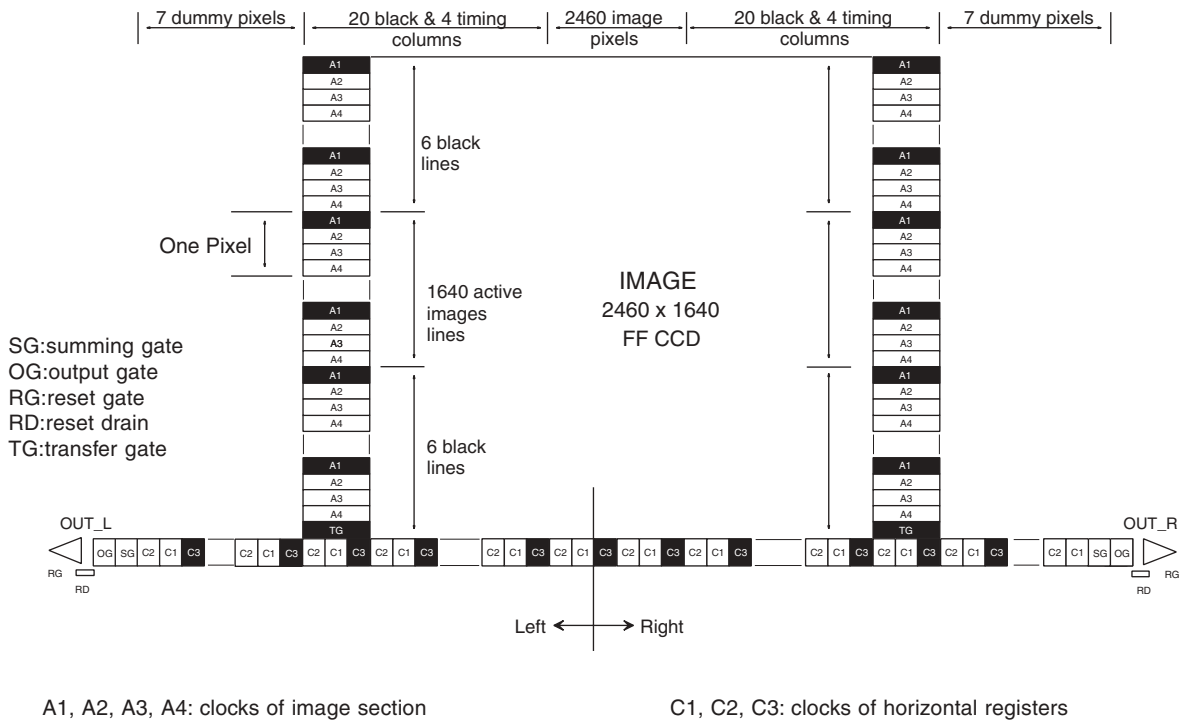


Figure 2 - Detailed internal structure

Specifications

ABSOLUTE MAXIMUM RATINGS[1]	MIN.	MAX.	UNIT
GENERAL:			
storage temperature	-40	+80	°C
ambient temperature during operation	-20	+60	°C
voltage between any two gates	-20	+20	V
DC current through any clock phase (absolute value)	-0.2	+0.2	µA
OUT current (no short circuit protection)	0	10	mA
VOLTAGES IN RELATION TO VPS:			
VNS, SFD, RD	-0.5	+30	V
VCS, SFS	-8	+5	V
all other pins	-5	+25	V
VOLTAGES IN RELATION TO VNS:			
SFD, RD	-15	+0.5	V
VCS, SFS, VPS	-30	+0.5	V
all other pins	-30	+0.5	V

DC CONDITIONS [2, 3]		MIN. [V]	TYPICAL [V]	MAX. [V]	MAX. [mA]
VNS[4]	N substrate	20	25.5	28	15
VPS	P substrate	1	6	7	15
SFD	Source Follower Drain	19	20	24	4.5
SFS	Source Follower Source	0	0	0	1
VCS	Current Source	-5	0	3	-
OG	Output Gate	2.0	2.5	4.5	-
RD	Reset Drain	19	20	21	-

AC CLOCK LEVEL CONDITIONS[2]	MIN.	TYPICAL	MAX.	UNIT
IMAGE CLOCKS / TRANSFER GATES [5]:				
A-clock amplitude during integration and hold	8	8	8.5	V
A-clock amplitude during vertical transport (duty cycle=5/8)[6]	11	11	11.5	V
A-clock low level	-	0	-	V
Charge Reset (CR) level on A-clock [7]	-5	0	-	V
OUTPUT REGISTER CLOCKS:				
C-clock amplitude (duty cycle during hor. transport = 3/6)	4.75	5	5.25	V
C-clock low level	2	4		V
Summing Gate (SG) amplitude		10	10	V
Summing Gate (SG) low level		tbd		V
OTHER CLOCKS:				
Reset Gate (RG) amplitude	4.5	5	5.5	V
Reset Gate (RG) low level	17	18	19	V
Charge Reset (CR) pulse on Nsub [7]	0	10	10	V

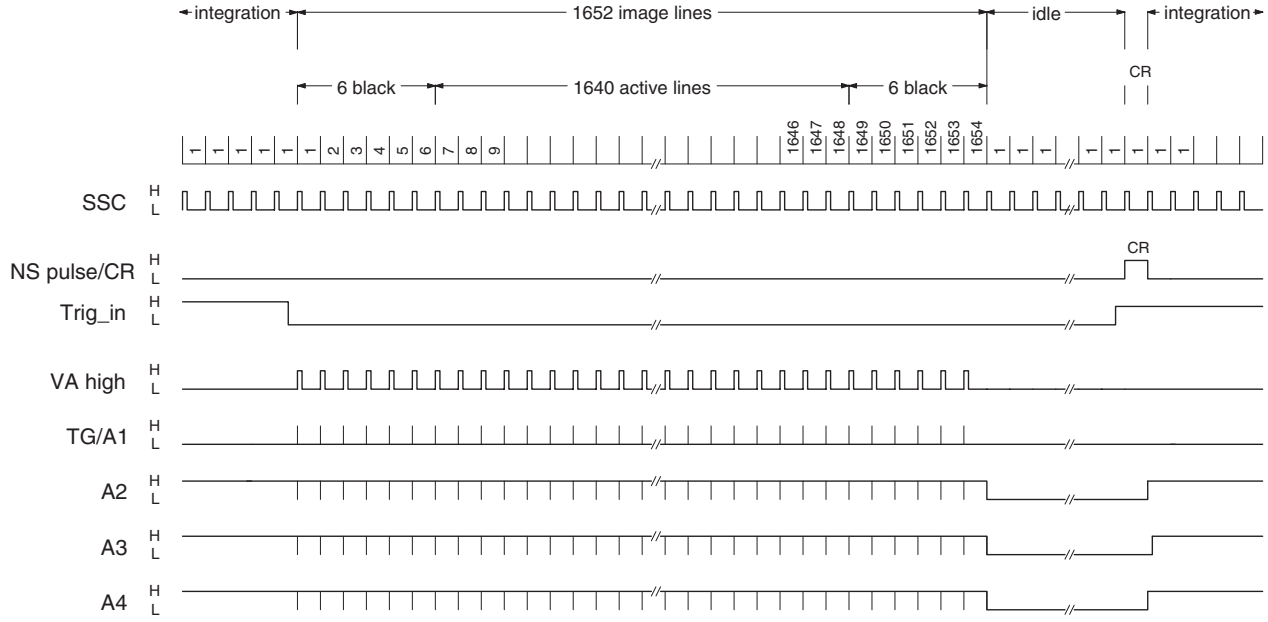
[1] During Charge Reset it is allowed to exceed maximum rating levels (see note [7]).
[2] All voltages in relation to SFS.
[3] Power-on sequence: VNS, SFD, RD, VPS, all others.
[4] To set the VNS voltage for optimal Vertical Anti-Blooming (VAB), it should be adjustable between minimum and maximum values.
[5] Transfer gate should be clocked as A1 during normal transport or held low during a line shift to sub-sample image.
[6] Three-level clock is preferred for maximum charge; the swing during vertical transport should be 3V higher than the voltage during integration. A two level clock (typically 10V) can be used if a lower maximum charge handling capacity is allowed.
[7] Charge Reset can be achieved in two ways:
- The typical A-clock low level is applied to all image clocks; for proper CR, an additional Charge Reset pulse on VNS is required (preferred).
- The minimum CR level is applied to all image clocks simultaneously.

Timing diagrams (for default operation)

AC CHARACTERISTICS		MIN.	TYPICAL	MAX.	UNIT
Horizontal frequency (1/Tp) [1]			25	27	MHz
Vertical frequency			75	150	kHz
Charge Reset (CR) time		10	Line time		µs
Rise and fall times:	image clocks (A)	10	20		ns
	register clocks (C) [2]	3	5	1/8 Tp	ns
	summing gate (SG)	3	5	1/8 Tp	ns
	reset gate (RG)	-	3	1/8 Tp	ns

[1] Tp = 1 clock period
[2] Duty cycle = 50%

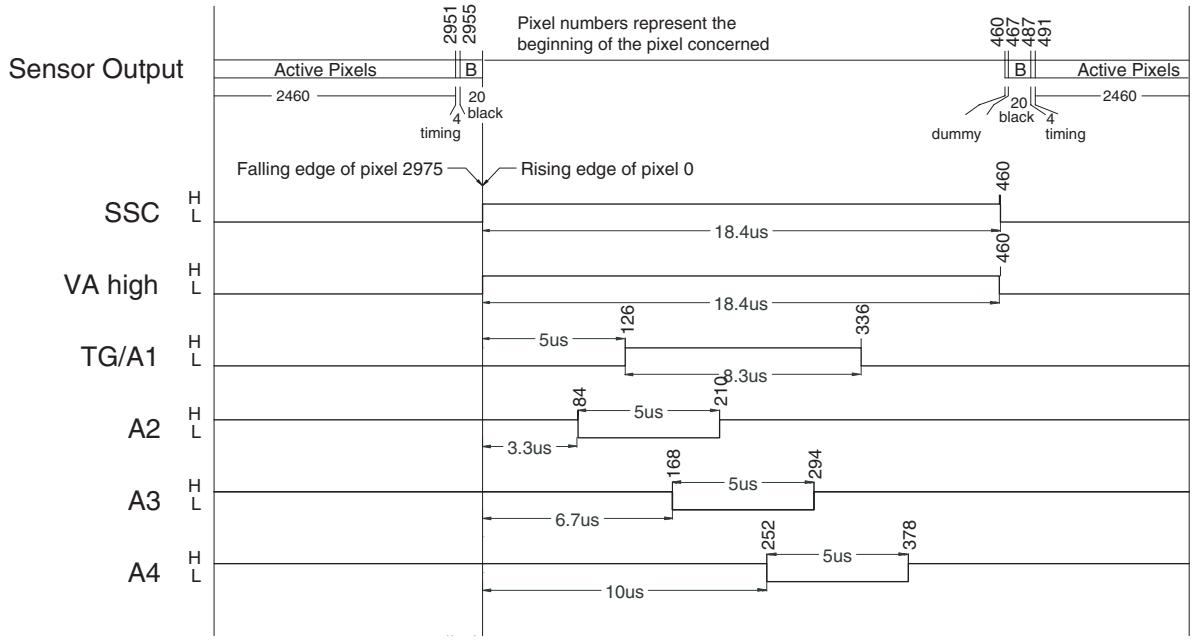
Frame timing



REMARKS
* CR is applied during the first line after the transition from L to H of Trig_in
* CCD is integrating during high period of Trig_in
* After read-out sequence the timing goes into idle mode.

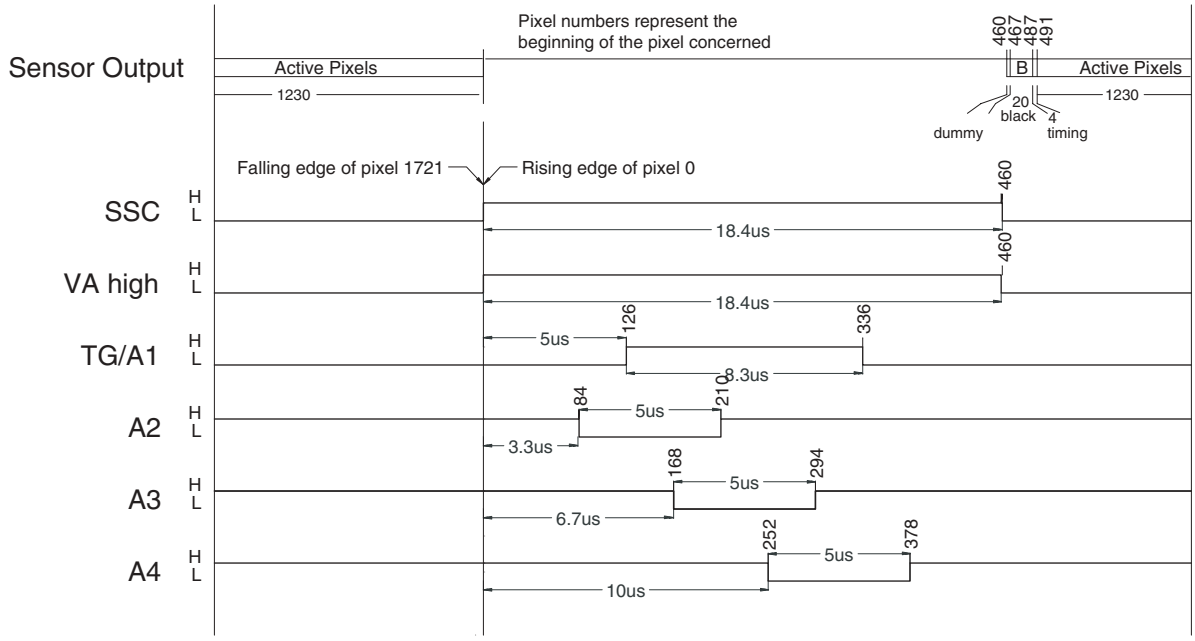
Figure 3 - Frame timing diagram

Line timing - single output



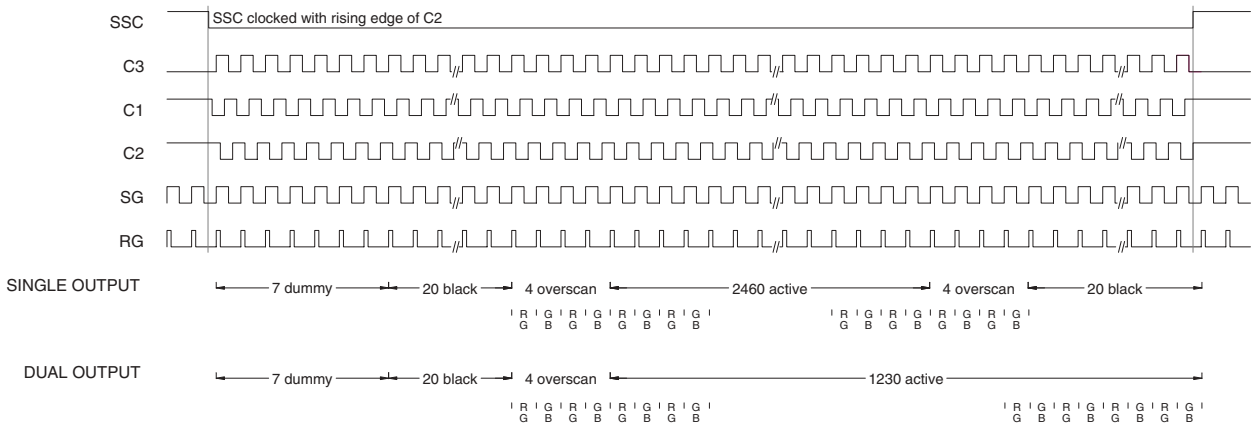
REMARKS
* Thorizontal = 2975 * 1/25E6 = 119us
* Vertical transport frequency = 75kHz

Line timing - dual output



REMARKS
* Thorizontal = 1721 * 1/25E6 = 68.84us
* Vertical transport frequency = 75kHz

Figure 4 - Vertical read-out, single and dual output modes



SENSOR PIN	C1L	C2L	C3L	C1R	C2R	C3R
SINGLE OUTPUT Left	C1	C2	C3	C1	C2	C3
SINGLE OUTPUT Right	C2	C1	C3	C2	C1	C3
DUAL OUTPUT	C1	C2	C3	C2	C1	C3

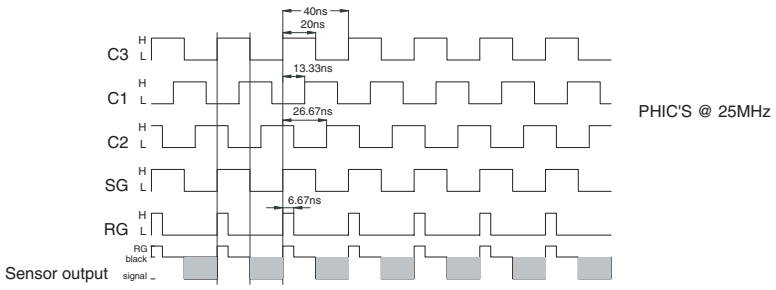


Figure 5 - Start horizontal read-out, single and dual output modes

Performance

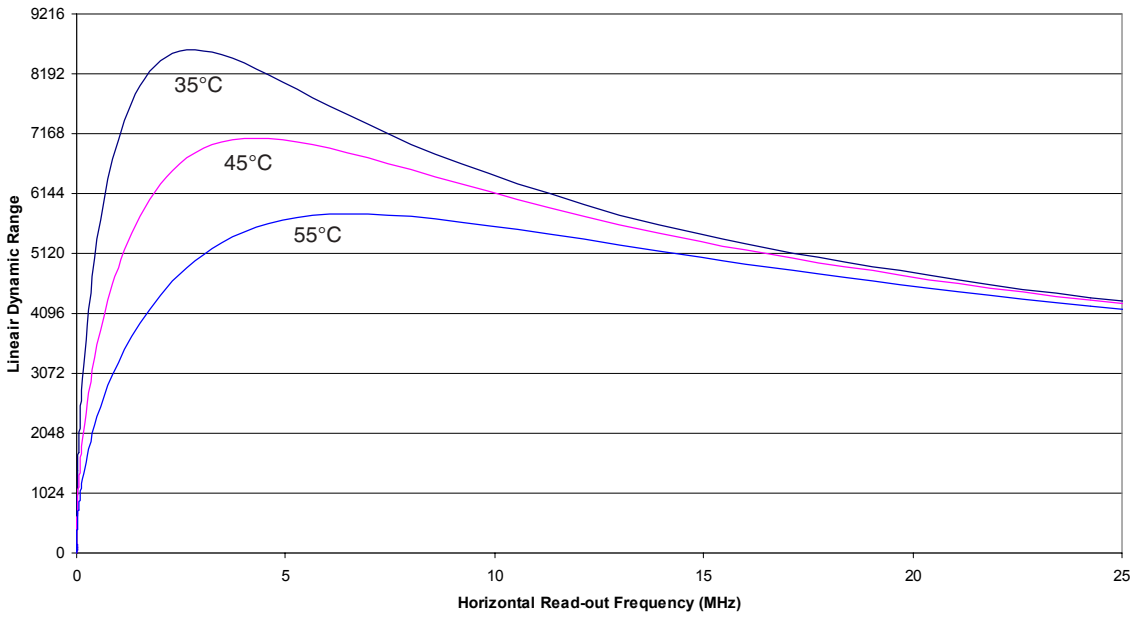
The test conditions for the performance characteristics are as follows:
- All values are measured using typical operating conditions.
- VNS is adjusted as low as possible while maintaining proper Vertical Anti-Blooming.
- Sensor temperature = 60°C (333K).
- Horizontal transport frequency = 25MHz.
- Vertical transport frequency = 75kHz.
- Integration time = 10ms.
- The light source is a lamp of 3200K in conjunction with neutral density filters and a 1.7mm thick BG40 infrared cut-off filter. For Linear Operation measurements, a temperature conversion filter (Melles Griot type no. 03FCG261, -120 mired, thickness: 2.5mm) is applied.

LINEAR OPERATION	MIN.	TYPICAL	MAX.	UNIT
Charge Transfer Efficiency [1] vertical		0.999995		
Charge Transfer Efficiency [1] horizontal		0.999999		
Image lag			0	%
Resolution (MTF) @ 56 lp/mm	65			%
Light sensitivity Green pixels @ 530nm	tbd	1000	tbd	mV/lux·s
Red/Green ratio	65	80	95	%
Blue/Green ratio	40	55	70	%
Low Pass Shading [2]		2	5	%
Random Non-Uniformity (RNU) [3]		1	5	%

[1] Charge Transfer Efficiency values are tested by evaluation and expressed as the value per gate transfer.

[2] Low Pass Shading is defined as the ratio of the one-σ value of an 8x8 pixels blurred image (low-pass) to the mean signal value.

[3] RNU is defined as the ratio of the one-σ value of the high-pass image to the mean signal value at nominal light.



Linear dynamic range is defined as the ratio of Q_{lin} to read-out noise with the read-out noise reduced by CDS.

Figure 6 - Typical Linear dynamic range vs. horizontal read-out frequency and sensor temperature

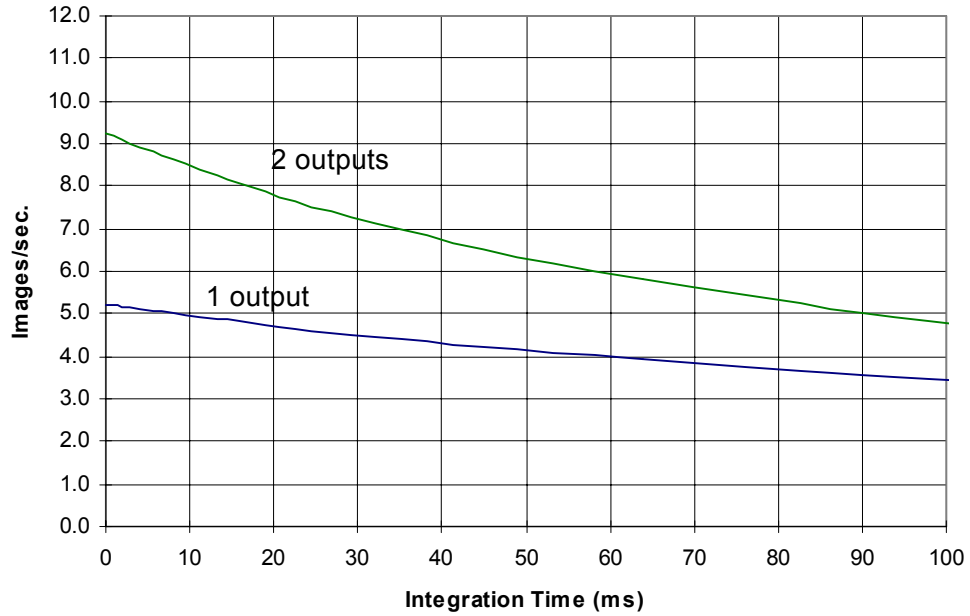


Figure 7 - Maximum number of images/second versus integration time

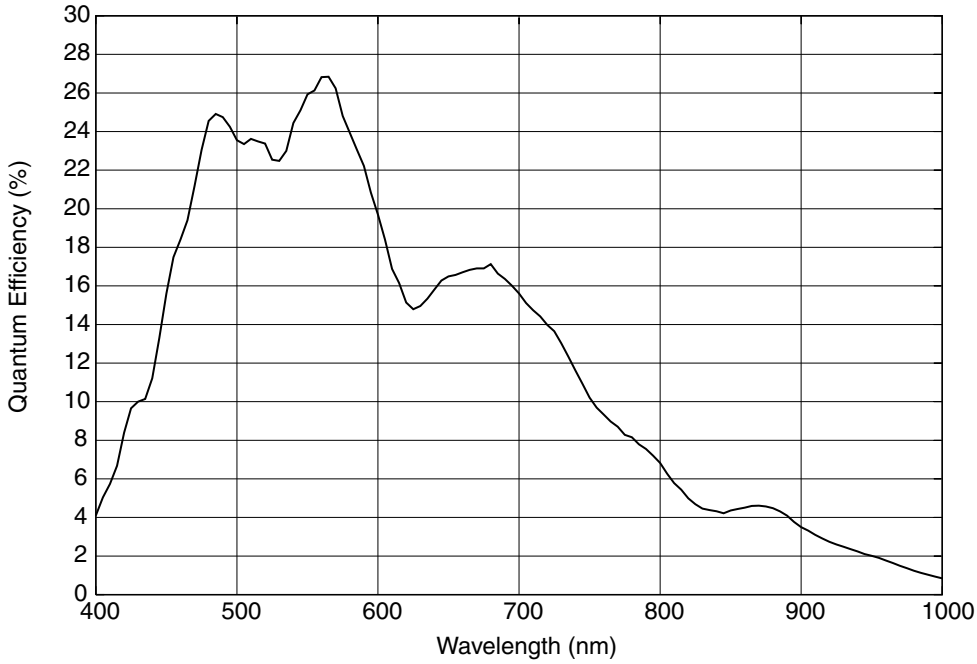


Figure 8 - Quantum efficiency versus wavelength

LINEAR/SATURATION	MIN.	TYPICAL	MAX.	UNIT
Full-well capacity saturation level (Qmax) [1]	tbd	tbd	tbd	mV
Full-well capacity linear operation (Qlin) [3]	tbd	tbd		mV
Charge handling capacity [4]		tbd		mV
Overexposure [5] handling		200		x Qmax level

[1] Qmax is determined from the low-pass filtered image.
[2] Qmax, shading is the maximum difference of the full-well charges of all pixels, relative to Qmax.
[3] The linear full-well capacity Qlin is calculated from linearity test (see dynamic range). The evaluation test guarantees 97% linearity.
[4] Charge handling capacity is the largest charge packet that can be transported through the register and read-out through the output buffer.
[5] Overexposure over entire area while maintaining good Vertical Anti-Blooming (VAB). It is tested by measuring the dark line.

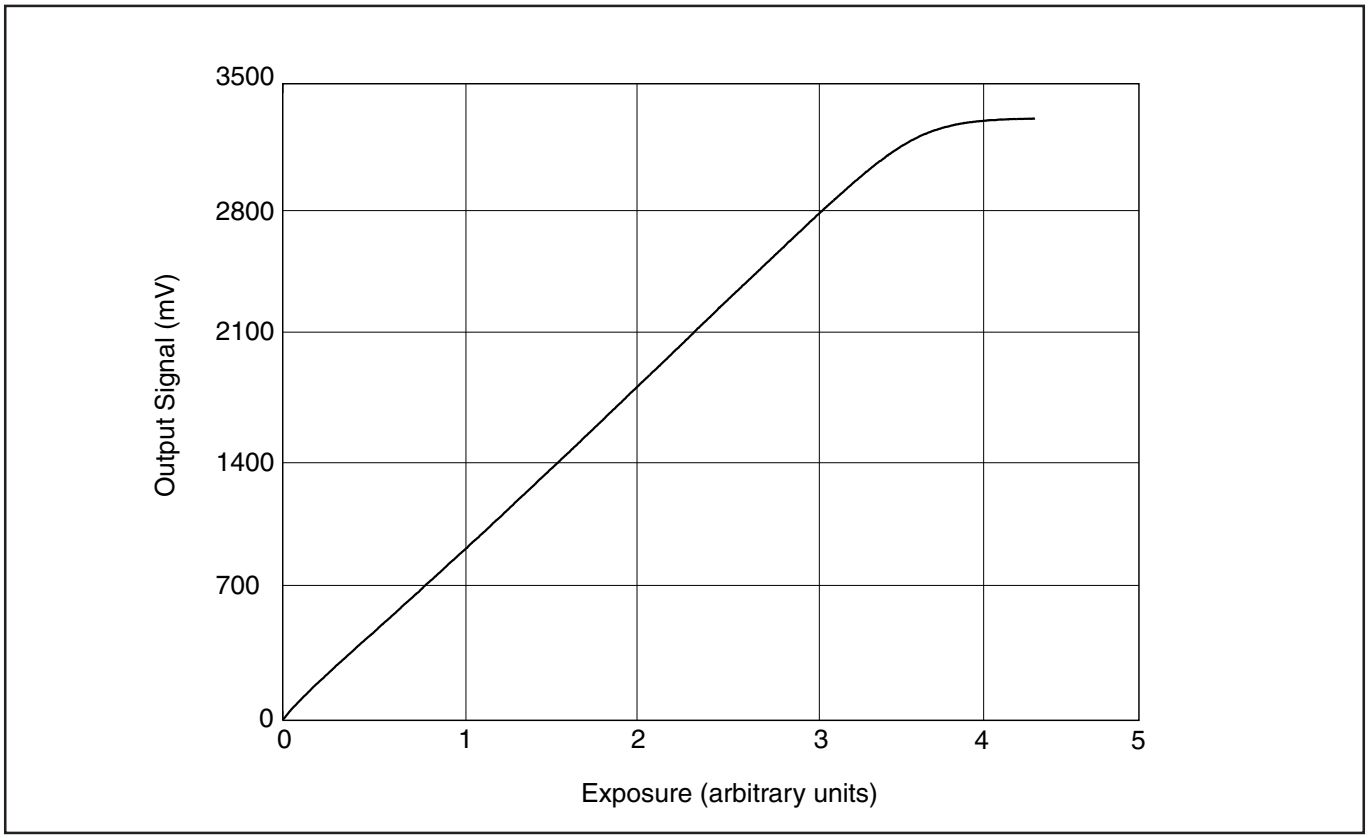


Figure 9 - Charge handling

OUTPUT BUFFERS	MIN.	TYPICAL	MAX.	UNIT
Conversion factor	32	35	38	µV/el.
Mutual conversion factor matching (ΔACF)[1]		0	2	µV/el.
Supply current		4.5		mA
Bandwidth (R_{load} = 3.3kΩ)	70	85		MHz
Output impedance buffer (R_{load} = 2.2kΩ, C_{load} = 2pF)		400		Ω

[1] Matching of the two outputs is specified as ΔACF with respect to reference measured at the operating point (Q_{lin}/2).

DARK CONDITION	MIN.	TYPICAL	MAX.	UNIT
Dark current level @ 20° C	-	10	30	pA/cm^2
Dark current level @ 60° C	-	0.3	0.6	nA/cm^2
Fixed Pattern Noise [1] (FPN) @ 60° C		15	20	mV
RMS system readout noise over full bandwidth after CDS		tbd	tbd	mV

[1] FPN is the one-σ value of the highpass image.

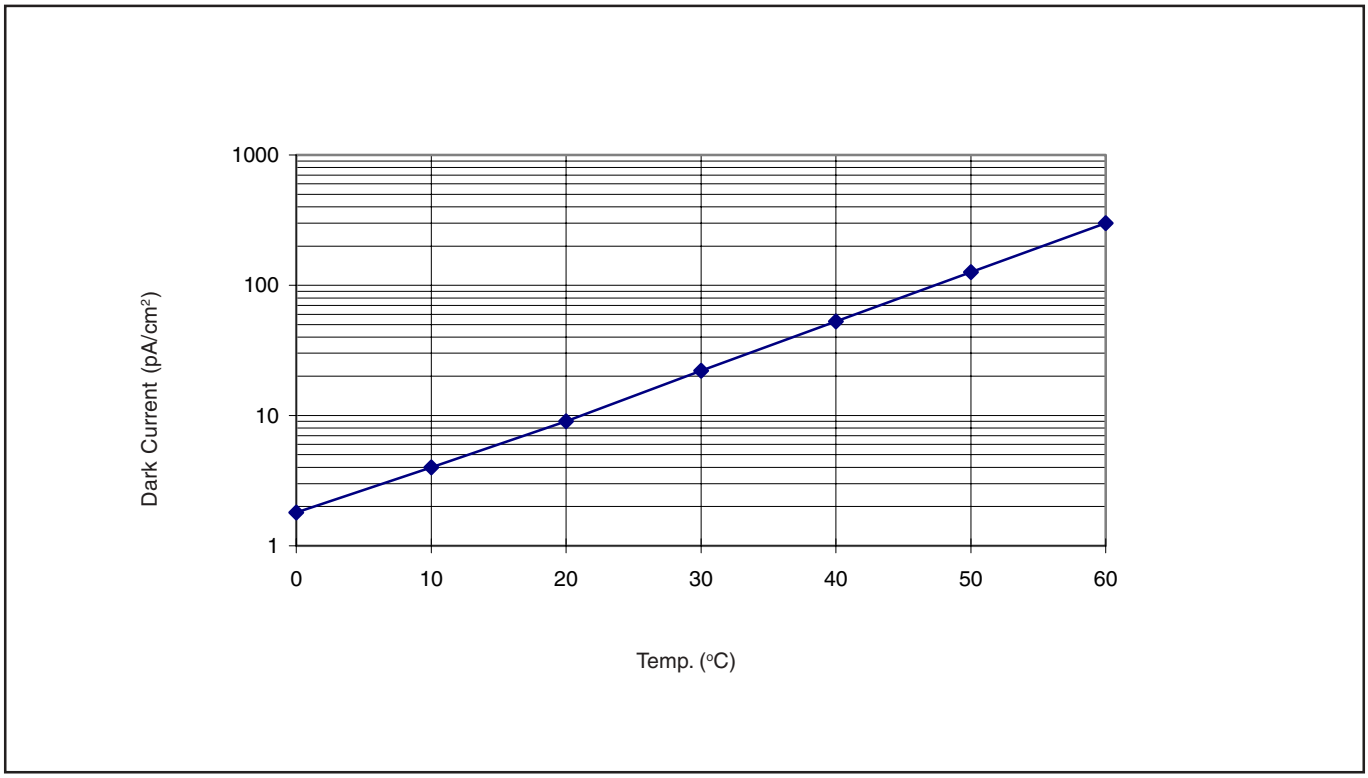


Figure 10 - Dark current versus temperature

Application information

Current handling
One of the purposes of VPS is to drain the holes that are generated during exposure of the sensor to light. Free electrons are either transported to the VRD connection and, if excessive (from over-exposure), free electrons are drained to VNS. No current should flow into any VPS connection of the sensor. During high overexposure a total current 5 to 10mA through all VPS connections together may be expected. The PNP emitter follower in the circuit diagram (figure 11) serves these current requirements.

VNS drains superfluous electrons as a result of overexposure. In other words, it only sinks current. During high overexposure a total current of 5 to 10mA through all VNS connections together may be expected. The clamp circuit, consisting of the diode and electrolytic capacitor, enables the addition of a Charge Reset (CR) pulse on top of an otherwise stable VNS voltage. To protect the CCD, the current resulting from this pulse should be limited. This can be accomplished by designing a pulse generator with a rather high output impedance.

Uncoupling of DC voltages
All DC voltages (not VNS, which has additional CR pulses as described above) should be uncoupled with a 22nF uncoupling capacitor. This capacitor must be mounted as close as possible to the sensor pin. Further noise reduction (by bandwidth limiting) is achieved by the resistors in the connections between the sensor and its voltage supplies. The electrons that build up the charge packets that will reach the floating diffusions only add up to a small current, which will flow through VRD. Therefore a large series resistor in the VRD connection may be used.

Outputs
To limit the on-chip power dissipation, the output buffers are designed with open source outputs. Outputs to be used should therefore be loaded with a current source or more simply with a resistance to GND. In order to prevent the output (which typically has an output impedance of about 400Ω) from bandwidth limitation as a result of capacitive loading, load the output with an emitter follower built from a high-frequency transistor. Mount the base of this transistor as close as possible to the sensor and keep the connection between the emitter and the next stage short. The CCD output buffer can easily be destroyed by ESD. By using this emitter follower, this danger is suppressed; do NOT reintroduce this danger by measuring directly on the output pin of the sensor with an oscilloscope probe. Instead, measure on the output of the emitter follower. Slew rate limitation is avoided by avoiding a too-small quiescent current in the emitter follower; about 10mA should do the job. The collector of the emitter follower should be uncoupled properly to suppress the Miller effect from the base-collector capacitance.
A CCD output load resistor of 3k3 typically results in a bandwidth of 85MHz.

Device protection
The output buffers of the FTF2416C are likely to be damaged if VPS rises above SFD or RD at any time. This danger is most realistic during power-on or power-off of the camera. The RD voltage should always be lower than the SFD voltage.

Never exceed the maximum output current. This may damage the device permanently. The maximum output current should be limited to 10mA.
Be especially aware that the output buffers of these image sensors are very sensitive to ESD damage.

Because of the fact that our CCDs are built on an n-type substrate, we are dealing with some parasitic npn transistors. To avoid activation of these transistors during switch-on and switch-off of the camera, we recommend the application diagram of figure 11.

Unused sections
To reduce power consumption the following steps can be taken. Connect unused output register pins (C1...C4, SG) and unused SFS pins to zero Volts.

Device Handling

An image sensor is a MOS device which can be destroyed by electro-static discharge (ESD). Therefore, the device should be handled with care.

Always store the device with short-circuiting clamps or on conductive foam. Always switch off all electric signals when inserting or removing the sensor into or from a camera (the ESD protection in the CCD image sensor process is less effective than the ESD protection of standard CMOS circuits).

Being a high quality optical device, it is important that the cover glass remain undamaged. When handling the sensor, use fingercots.

When cleaning the glass we recommend using ethanol (or possibly water). Use of other liquids is strongly discouraged:

- if the cleaning liquid evaporates too quickly, rubbing is likely to cause ESD damage.
- the cover glass and its coating can be damaged by other liquids.

Rub the window carefully and slowly.

Dry rubbing of the window may cause electro-static charges or scratches which can destroy the device.

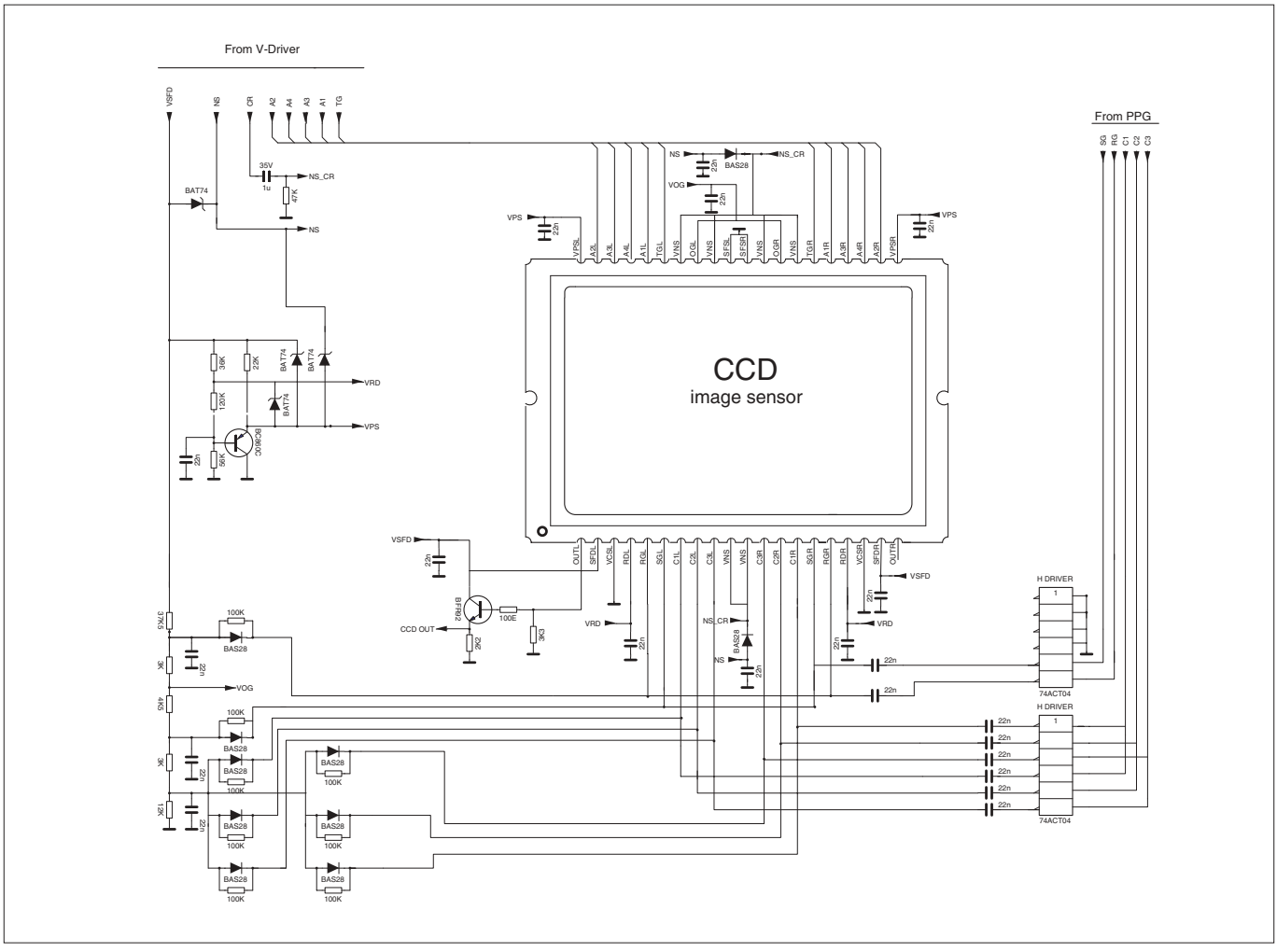


Figure 11 - Application diagram for single output operation

Pin configuration

The FTF 2416C is mounted in an LCC package with 40 pins (20 each side).

Symbol	Name	Pin # (Out_L)	Pin # (Out_R)
OUT	Output	1	20
SFD	Source Follower Drain	2	19
VCS	Voltage Current Source	3	18
RD	Reset Drain	4	17
RG	Reset Gate	5	16
SG	Summing Gate	6	15
C1	Register Clock (1)	7	14
C2	Register Clock (2)	8	13
C3	Register Clock (3)	9	12
A1	Image Clock (1	36	25
A2	Image Clock (2)	39	22
A3	Image Clock (3)	37	24
A4	Image Clock (4)	38	23
TG	Transfer Gate	35	26
OG	Output Gate	33	28
SFS	Source Follower Source	31	30
VPS	P Substrate	40	21
VNS	N Substrate	10, 32, 34	11, 27, 28

Notes:
- Pin 1 has a small dot next to the lead.
- "open" bond pads must be left unconnected. They are currently tied to VNS in the silicon, but this may change in the future.

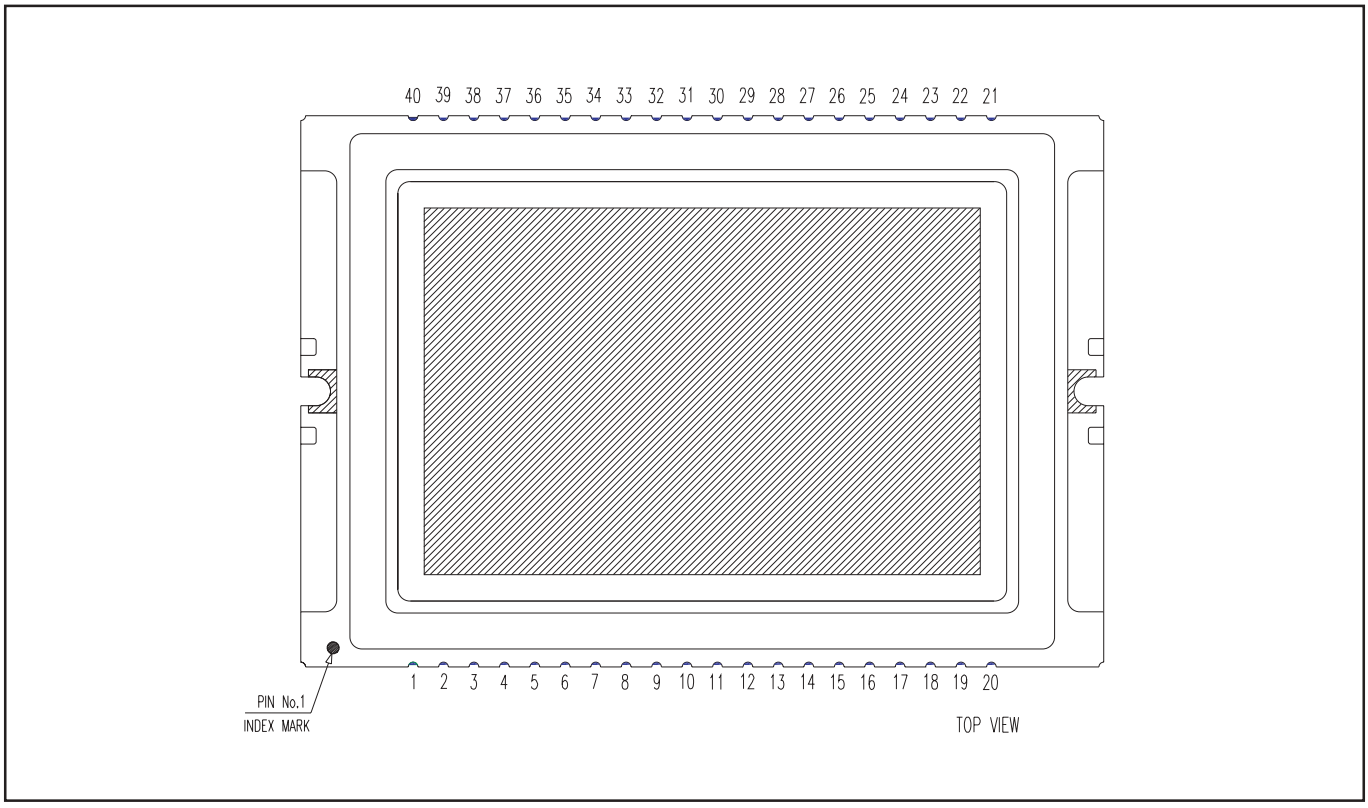
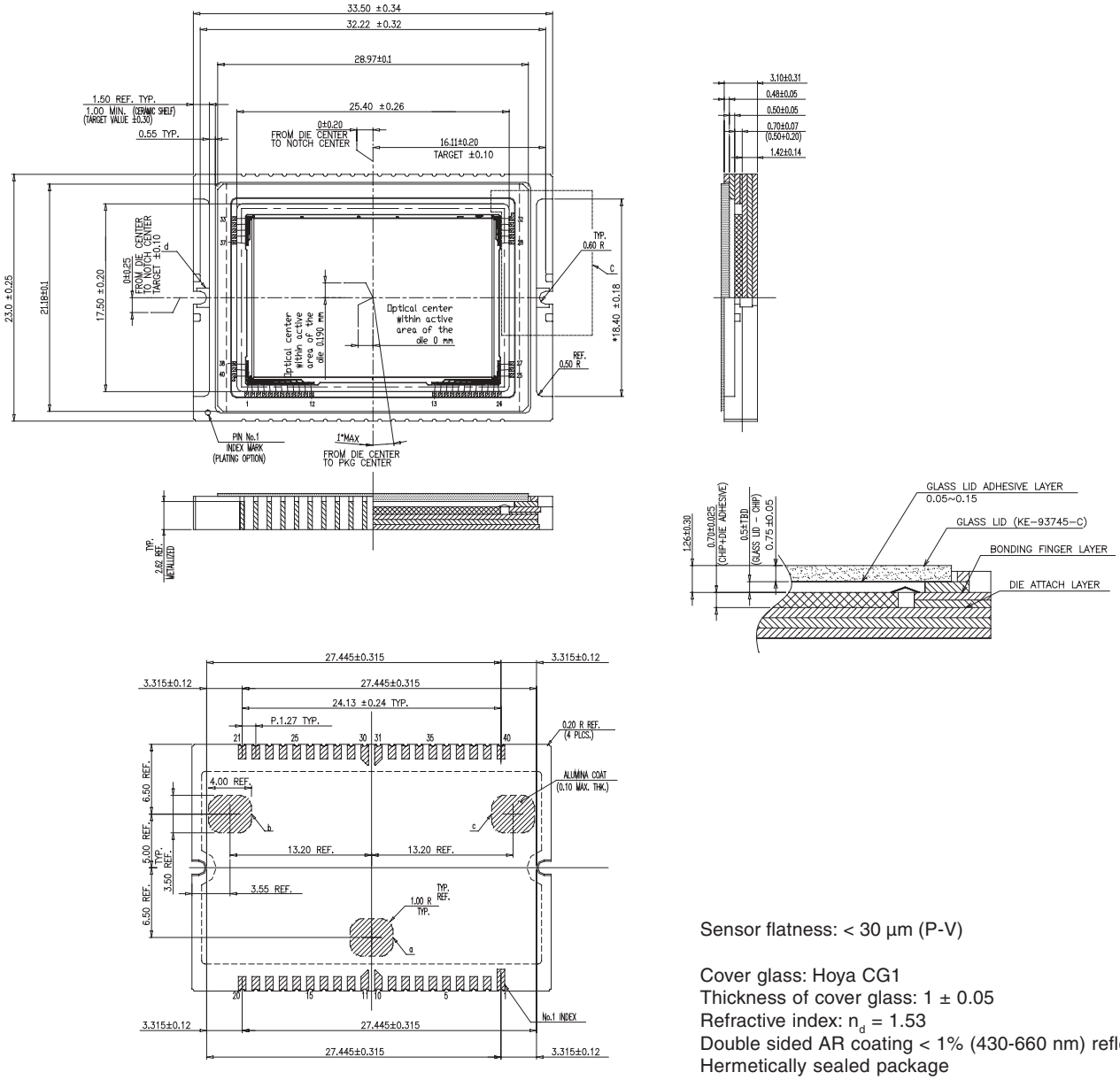


Figure 12 - Pin configuration (top view)

Package information



Sensor flatness: < 30 µm (P-V)

Cover glass: Hoya CG1
Thickness of cover glass: 1 ± 0.05
Refractive index: n_d = 1.53
Double sided AR coating < 1% (430-660 nm) reflection
Hermetically sealed package

All drawing units are in mm

Figure 13 - Mechanical drawing of the PGA package

Order codes

The sensor can be ordered using the following code:

FTF2416C sensor		
Description	**Quality Grade**	**Order Code**
FTF2416c	Test grade	xxxx xxx xxxx

You can contact DALSA Professional Imaging at the following address:

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