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Detection of visible photons in CCD and CMOS: A comparative view

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Abstract

CCD and CMOS detectors each have strengths and weaknesses coming from their architecture or their fabrication process. This paper reviews their key architectural and technological differences that impact the photon detection performances and gives the future directions for CMOS detectors evolution.

Keywords: CCD; CMOS; Detectors

1. Introduction

The Charge-Coupled Device (CCD) has been the dominant technology for visible photon detection and image capture over the last two decades due to its ability to perform very efficiently and uniformly over large areas, the collection and transfer of generated charges and its measurement at low noise. But thanks to the past 10 years intensive work [1–3], maturity of the CMOS detectors is now established and the advantages of their specific features, allowed by the in-pixel amplification, column-parallel architecture and the use of deep sub-micron CMOS processes, are currently used in several applications. Following the replacement for infrared focal plane array readout of CCD by CMOS multiplexers in the late 1980s, a move from CCD to CMOS for the visible photons detection can be observed, obviously not only for low-cost imaging markets but also for many high performances applications such as high-end Digital Still Photography [4], High-Definition Television [5] and several space applications [6]. After a review of the main architectural differences between CCD and CMOS that explains the noise behavior difference, Quantum Efficiency (QE) will be compared with reference to technological characteristics. A brief survey of CCD state-of-the-art will then be given and perspectives for the future CMOS detectors will be drawn.

2. From photon to electrical signal in CCD and CMOS approaches

CCD and CMOS devices used for photons detection are organized as arrays of photodetectors that deliver an electrical signal related to the amount of photons that fall on the pixel surface during the integration time. They both use the photoelectric effect in silicon, in either a photogate or a photodiode detector.

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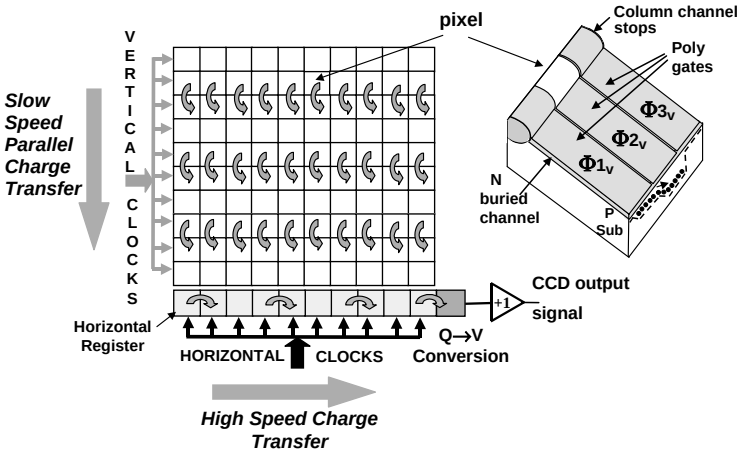

Fig. 1. CCD architecture (full-frame organization).

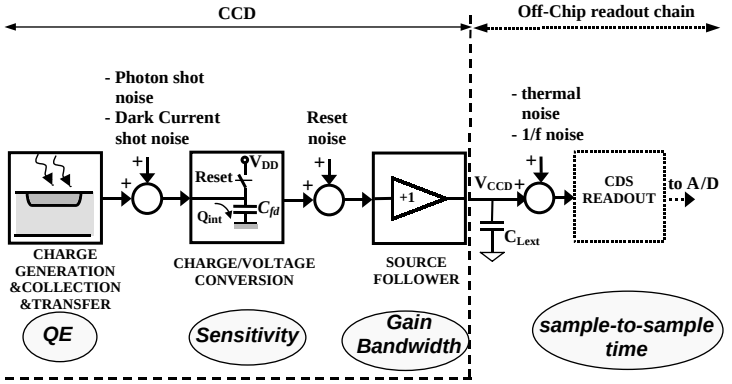

Fig. 2. From photons to signal digitization in CCDs.

2.1. The CCD organization

In the well-known CCD approach recalled in Fig. 1, photoelectrons are transported in the charge domain through vertical (parallel) and horizontal (serial) buried channel CCD shift-registers to a single readout node where charge-to-voltage conversion is performed (commonly by "floating diffusion" technique). Fig. 2 summarizes the processes involved from photon interaction with silicon to signal digitization and the key parameters that impact these steps: QE, Sensitivity (or conversion factor), gain and bandwidth of Source Follower (SF) amplifier. QE-related aspects will be discussed later in a comparative way with respect to the CMOS one.

The sensitivity is $S_v = G_{SF}(q/C_{fd})$ (generally expressed in μV/e) with q: electron charge, C_{fd} total capacitance of the sense node and G_{SF} is the SF gain (often 0.8–0.9). A high sensitivity value, in the range of 5–10 μV/e, is desirable in order to get a small input referred noise given by $NEQ = \sqrt{\sigma^2_{V_{CCD}}}/S_v$ where $\sigma^2_{V_{CCD}}$ refers to the total noise power measured at the output, thus implying a very small sense node capacitance. A somewhat tedious optimization of the SF is required in order to minimize its input capacitance that has to be

balanced with signal output drive capability and settling times of video signal V_{CCD}.

The SF is necessarily wideband in order to allow the double sampling process to occur in one pixel time frame with a complete settling of the signals. Thus, in CCD, the bandwidth noise shaping is performed at video rate. Fig. 2 gives also a representation of the most important noise sources in CCD: photon shot noise, due to the random arrival of photons on the detector, is unavoidable and produces $\sqrt{N_{Sig}}$ rms noise electrons if N_{Sig} represents the amount of collected photoelectrons during the integration ($N_{Sig} = QE\, N_{Ph}$ where QE is the quantum efficiency and N_{Ph} is the number of impinging photons) and the dark current (DC) shot noise is given in rms electrons by $\sqrt{N_{DC}}$ if the DC charge is N_{DC}. It can only be minimized by reducing the DC density using inverted mode (Multi Phased Pinned–MPP) or cooling. Thanks to the use of buried channel, the transfer noise in CCD is nowadays negligible. The CCD output signal V_{CCD} contains the readout diffusion reset noise (rms voltage $\sigma_{Reset} = \sqrt{KT/C_{fd}}$ or $N_{\boldsymbol{Reset}} = (1/q)\sqrt{KTC_{fd}}$ in rms electrons), the thermal and $1/f$ components of the SF transistor noise.

The external Correlated Double sampling (CDS) readout processor perform a differential double sampling of the reset and signal levels [7] whose effects are:

- to eliminate the reset noise of the floating diffusion;
- to filter the SF noise PSD.

The CDS both acts as a High pass filter for the $1/f$ noise (transfer function $|H(f)|^2 = 4\sin^2(\pi f\, T_D)$), where T_D is the sample-to-sample time (here the time allowed for charge transfer in C_{fd} after the reset switch is opened) and limits the effect of the white noise to a cutoff frequency f_c that has to be compatible with the pixel readout rate f_{pix}.

Thus in CCD, if CDS is performed (off-chip), the read noise is dominated by the SF MOS white noise in the frequency band limited by f_c, and the noise bandwidth is determined by the video output signal rate $f_{video} = 2X_C\, Y_R f_{frame}$, where f_{frame} is the frame rate, X_C is the number of columns, and Y_R is the number of rows. So for significant size of array and frame rate, the noise bandwidth is fixed to several MHz or even several tens MHz (except for very low scan rates as in astronomy) leading to few tens of noise electrons taking into account state-of-the-art conversion capacitance value around 8–10 fF and external load capacitance in the order of 10 pF [8].

2.2. *Benefits of CMOS active pixel sensors architecture*

The main contribution of CMOS active pixel sensors is the combination inside the pixel of the detector, the charge-to-voltage conversion and transistors providing buffering and addressing capability. This unique feature allows for a memory-like organization, shown in Fig. 3, where most of the operations are performed in the voltage domain. A parallel sampling at low rate of a whole pixel's row signals and the multiplexing of column signals are performed at the bottom of the array, giving a row-based readout mechanism. This organization, in contrast to CCD architecture, provides random access to pixel and direct windowing capability at a very high frame rate and avoids the multiple charge transfers over long distances of the CCD architecture that are very sensitive to radiation degradation. The devices can make use of CMOS fabrication process based on high diffusion digital and mixed signal process (memories, μP, telecom, etc.) using low power supply levels (5–3.3 V) that provide low power dissipation (50–100 mW) and the capability of integrating of peripheral functions (dedicated timing and control for example) as shown in Fig. 4 and a way of developing non-standardized detectors (detector ASIC). To allow detection of low flux level, most of CMOS sensors operate in charge integrating mode and both photogate (associated with a transfer transistor) or photodiode can be used for photon detection [9] (Fig. 5). In the first case, charge-to-voltage conversion is performed by a small readout diffusion independent of pixel size thus providing high conversion gain (CVF) value (up to 30 μV/e^-). Photodiodes are often used in self-integrating mode thus performing charge-to-voltage conversion on the detector capacitance itself (3T pixel) with CVF

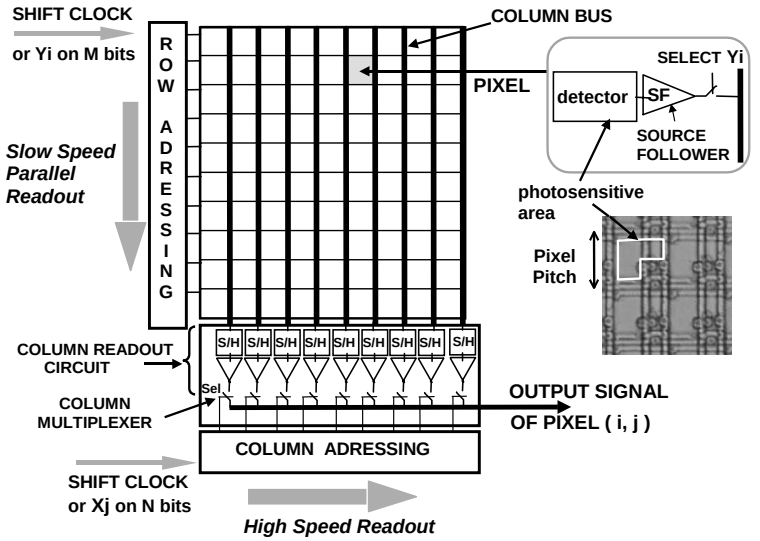

Fig. 3. CMOS APS architecture.

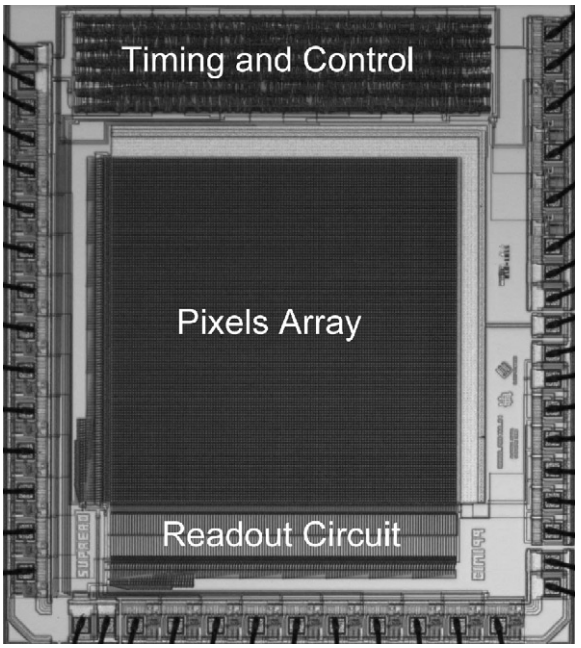

Fig. 4. Example of peripheral functions integration capability in CMOS detectors.

being dependent on photodiode area and usually limited to 1–4 μV/e$^-$ depending on pixel size. Derived from Infrared readout circuits, fixed bias photo-current integration using CTIA can also be used in order to get the same sensitivity value as photogate [10].

Fig. 6 provides a representation of the various steps involved in the process of producing output signal from photons in CMOS detectors and most important noise sources associated with them. An important difference between CCD and CMOS in the read noise behavior due to the architecture should be noticed: in contrast to CCD where noise is captured at the highest bandwidth (at the output), due to the column-parallel organization of CMOS arrays, the noise bandwidth is set to the row readout bandwidth by the bottom column sampling circuitry that filters the in-pixel SF noise. It has been shown [11] that the in-pixel SF transistor (M_{SF} in Fig. 5) thermal noise is the major noise contributor if CDS readout (being on-chip in that case) is applied and that minimization through careful design and layout can be obtained. It follows that, in contrast to CCD where noise increase with video frequency, the noise of CMOS detector is relatively independent of the video rate [8]. However, Fill-Factor and pixel size constraints limit the optimization margins of the in-pixel SF while the column sampling and multiplexing circuitry (vertically aligned in the pitch) is unconstrained in one dimension. The removal by CDS readout mode of both $1/f$ noise of the

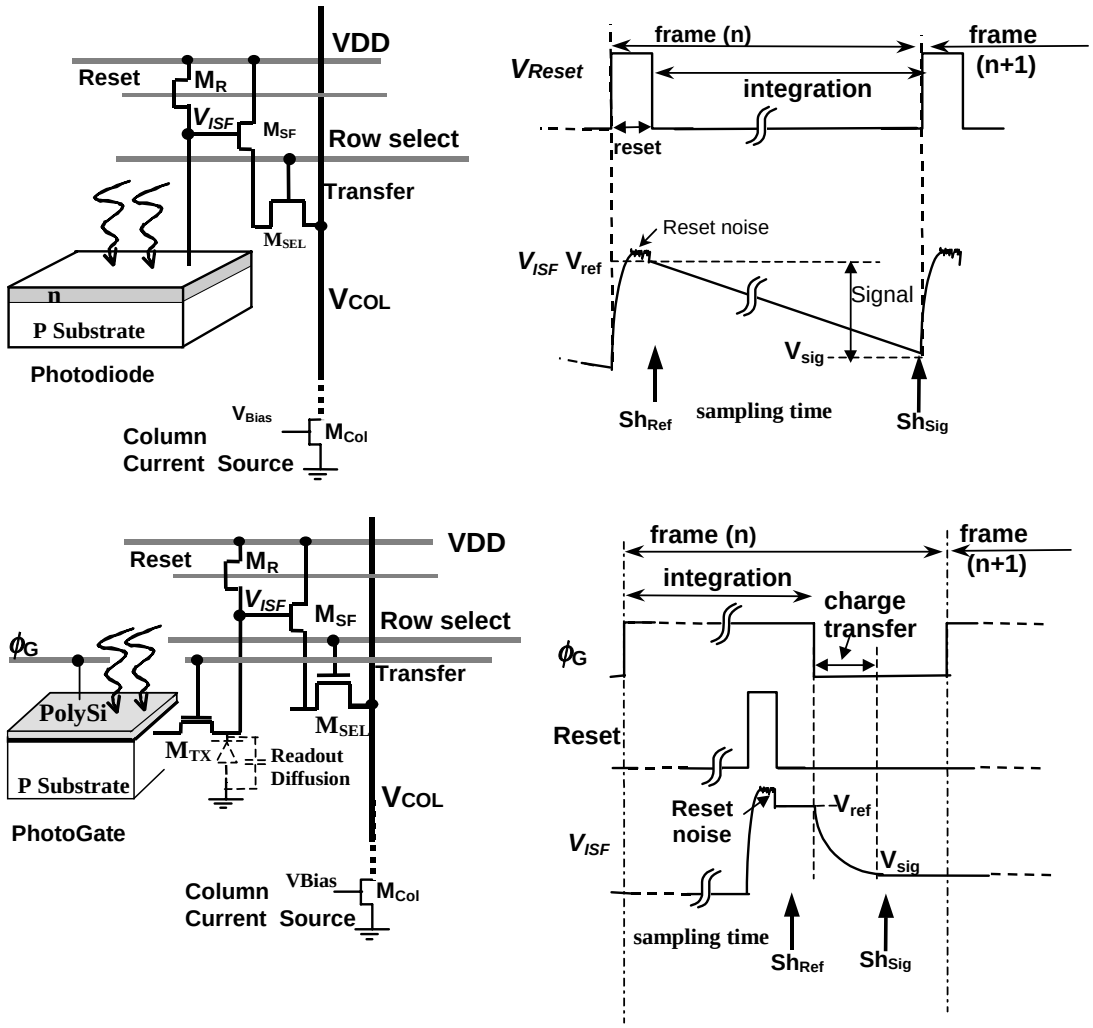

Fig. 5. Two types of CMOS detectors used in integration mode: photodiode and photogate.

in-pixel source-follower MOSFET and KTC sense node noise requires separate detection and conversion nodes. It can easily be obtained with photogate pixel as soon as the sample-to-sample time (i.e. the transfer time) is of short duration, in the range of a few μs. But in the classical 3T photodiode pixel, the photodiode KTC noise cannot be easily removed without the use frame-memory or additional in-pixel circuitry that reduces photosensitive area [12] and is usually the dominant contribution if the detection area is significant, thus giving the photogate pixel a superiority in terms of dynamic range. If separate detection and conversion nodes are used, adoption of deep sub-micron process allows the implementation of very small sense capacitance (a few fF) and gives access to S_v values up to $50\,\mu V/e^-$, leading to a few of noise electrons when considering the typical range (100–200 μV) of readout noise voltage at the output. So taking into both account noise bandwidth and conversion gain, CMOS detection arrays have the potential of being superior to CCD in terms of read noise [13].

Regarding DC and DC shot noise, very strong improvement have been done at the CMOS

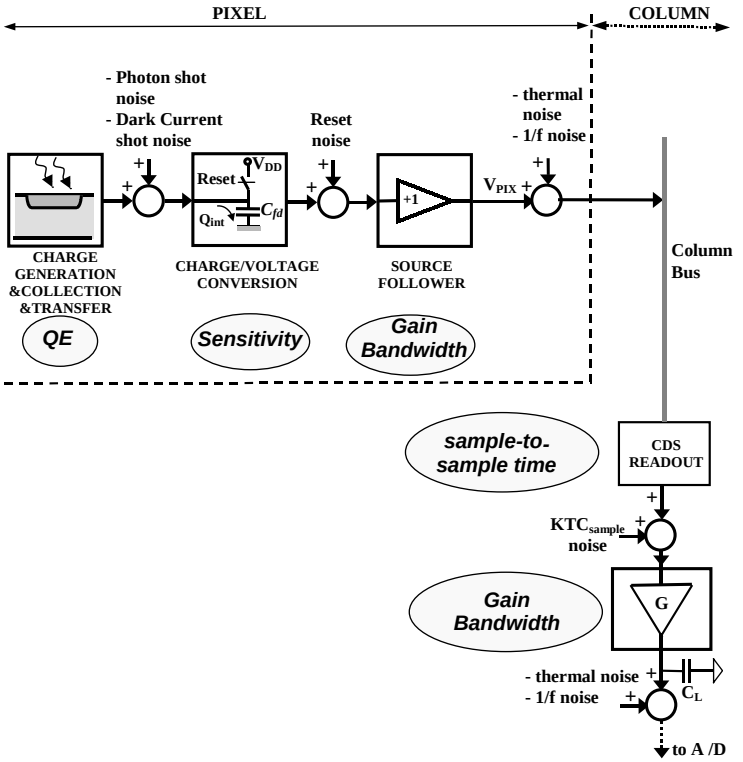

Fig. 6. From photons to signal digitization in CMOS detectors.

foundry level and allow typical DC range value from 0.5 to 1 nA/cm^2 for very standard CMOS process, and from 50 to 200 pA/cm^2 for optimized process, associated with very good uniformity as indicated in Fig. 7 that gives a DC map of a CMOS detector (512×512 pixels) developed by SUPAERO on a standard CMOS process [14] have been allowed.

The anti-blooming behavior of CMOS APS is naturally good as demonstrated in Fig. 8 without additional degradation of Fill-Factor.

Radiation tolerance of CMOS detectors arrays has been demonstrated to be very good due to the architecture and the use of deep sub-micron processes, several tens of Krad for standard design and process to more than 1 Mrad for radiation hardened design and foundries [15]. The evolution to deeper sub-micron CMOS process allows to be confident in the potential improvements of the radiation tolerance of the devices.

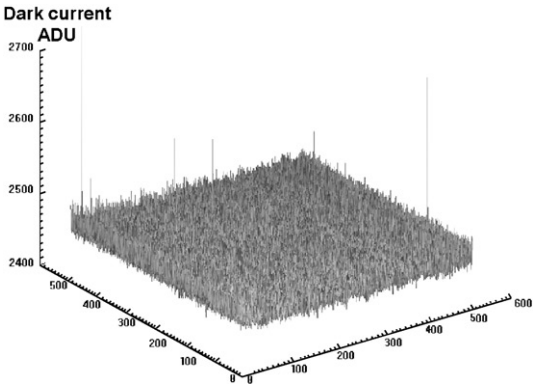

Fig. 7. DC map of a 512×512 pixel detector demonstrating very good uniformity.

3. Comparative view of CMOS and CCD quantum efficiency

CCD and CMOS detectors share several common aspects in terms of QE and both are being

manufactured in monocrystalline silicon, using photoelectric effect for electron–hole pair generation and electric field for carrier separation. Due to different fabrication targets, CCD and CMOS devices differ strongly in both composition and thickness of top layers, and space charge region depth and doping as shown in Fig. 9. Incident visible photons in both devices have to go through a stack of top layers before being absorbed by silicon. Due to the different refractive indexes (Si:3–5; SiO2:1.45), thickness and nature of the various materials used in this stack, transmission will be limited and wavelength dependent. Fig. 10 gives the simulated transmission curves (by transmission matrix method) of two standard CMOS processes of different generations using real process data. As a general trend, transmission is getting more complex as technology is shrinked due to the multiple levels of interconnections and interlayer dielectrics (ILD) that are used (0.5 μm:3 metal layers; 0.35 μm:4 metal layers; 0.25 μm:5 metal layers; 0.18 μm:6 metal layers). The CCD top-level structure is in any case simpler and can be optimized for high transmission value. However, remarkable improvements in the transmission losses of CMOS detector have been obtained, for example through the use of near-surface antireflection layers [16], by CMOS foundries interested in the imaging market that have developed dedicated process modules for high performance detector compatible with the core mixed signal process.

Fig. 8. Natural CMOS anti-blooming behavior demonstration (the two gray spots response is at mid-dynamic range level while the white one is over saturated).

Due to some "optically dead" area, such as anti-blooming structure (Lateral Overflow Drain-LOD) in CCD or active transistors and metal lines in CMOS, some of the incoming photons will be inefficient in generating collectible electrons. In that case, one can define an effective QE as Effective_QE = Fill_Factor.Physical_QE where the Physical QE is defined as the ratio (Number of collected electrons)/(Number of incident photons) of a detector area whose area is entirely photosensitive.

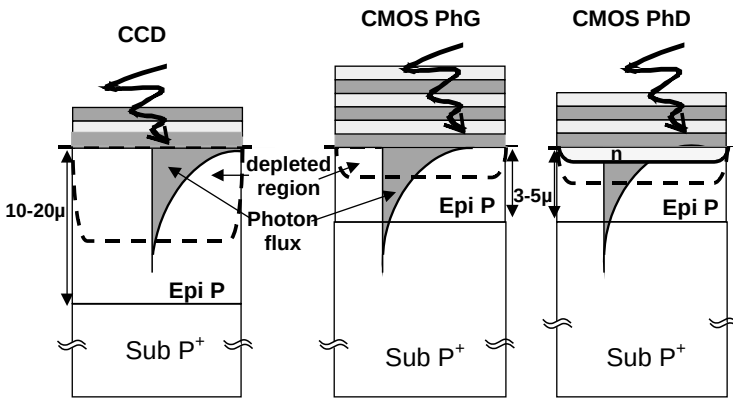

Fig. 9. Comparison of CCD and CMOS photodiode and photogate detector cross-sections demonstrating differences in both top layers structure and depth of space charge regions in silicon.

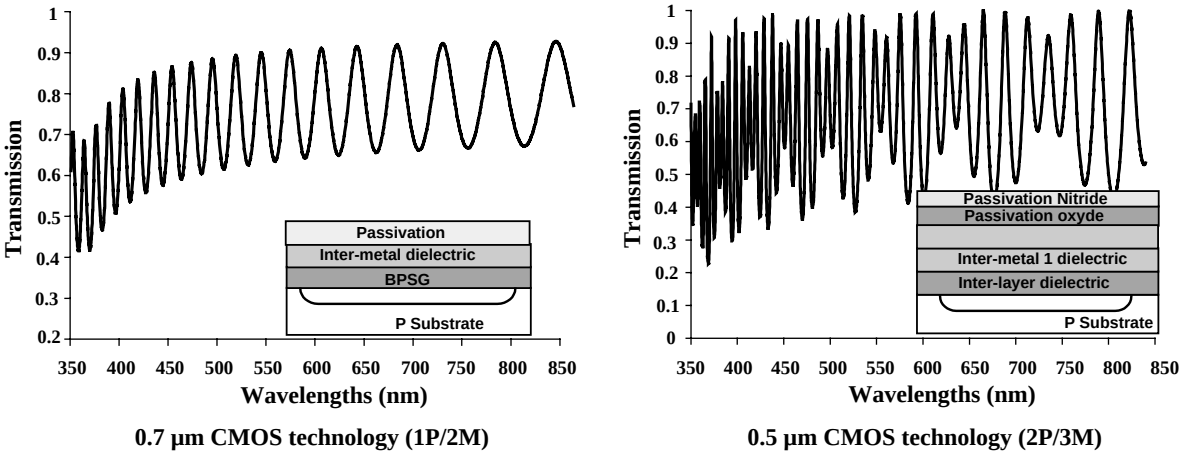

Fig. 10. Simulated transmission of top layers stack in two CMOS process generations: a simple two metal layers 0.7 µm and a three metal layers 0.5 µm.

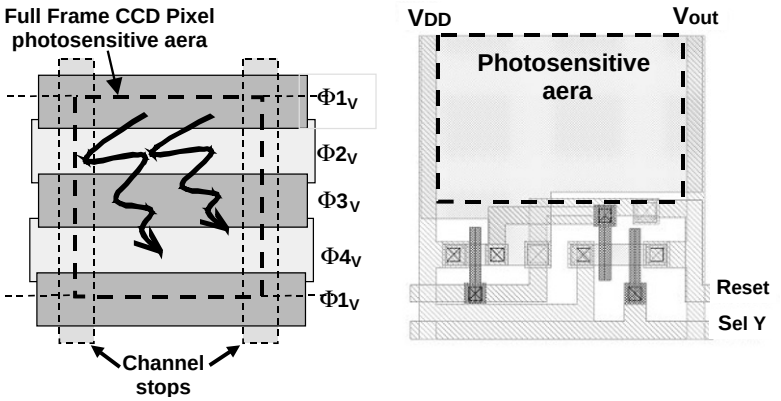

Fig. 11. Top view of a full-frame non-LOD CCD pixel demonstrating 100% Fill-Factor and a CMOS photodiode pixel (8 µm) having 55% Fill-Factor.

This attributes an important role to Fill-Factor. Fig. 11 compares the situation of a full-frame CCD without lateral anti-blooming drain and CMOS (here photodiode) small pitch (8 µm) pixel by giving, respectively, a symbolized top view and real possible layout view. The CMOS pixel (having nearly 55% Fill-Factor) appears penalized but two remarks have to be done: first, this example has been chosen in order to demonstrate the nature of non-photosensitive area but is only realistic for small pixel pitch. Fig. 12 gives a real microphotograph of a 20 µ pitch pixel in 0.5 µm process that shows a very large photosensitive area and the transistors area covered by metal lines. Thus with deep sub-micron process, very high Fill-Factor can be achieved for mid-range pixel pitch (above 10 µm). Secondly, in the CCD case, the presence of a lateral anti-blooming drain will imply a reduction of the Fill-Factor resulting in severe loss in QE by the effect of the depletion regions generated by the LOD biasing. A comparison of QE curves for a commercial traditional poly-gates CCD (Kodak KAF 6303) and a prototype photogate CMOS array (designed at SUPAERO) featuring 56% Fill-Factor and fabricated using a 0.5 µm standard process (AMIS) is given in Fig. 13. It demonstrates that the curve for the CMOS photogate (that benefits of a natural anti-

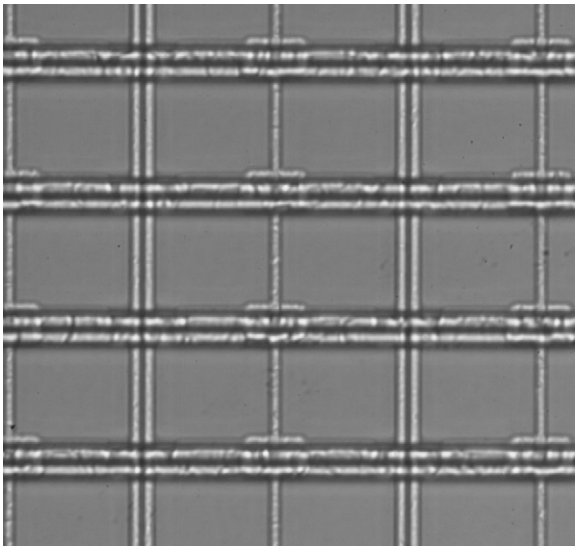

Fig. 12. Microphotograph of a 20 μm pitch pixel in 0.5 μm process showing large photosensitive area.

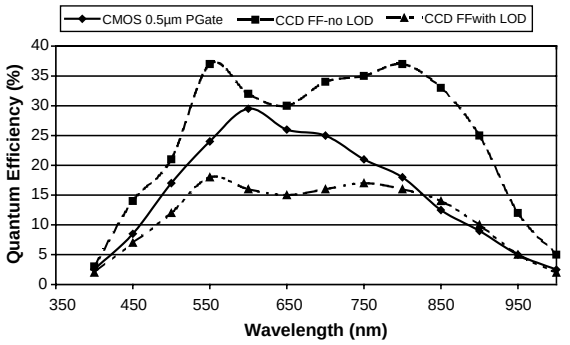

Fig. 13. Comparison of QE of traditional poly-gates LOD and no-LOD CCDs (Kodak 6303) and CMOS photogate array (56% Fill-Factor; standard 0.5 μm CMOS process).

blooming behavior) is above the CCD with LOD, even with its limited Fill-Factor and that with the improvement in Fill-Factor coming from scaled design rules, it can compete with traditional frontside poly-gates. However, both devices suffer from poor QE at short wavelength.

The second important aspect in QE comparison is charge collection efficiency [17]. It is related to both active layers thickness in silicon, substrate doping profile, carrier lifetime and voltage drive levels. As indicated in Fig. 9, CCD technologies

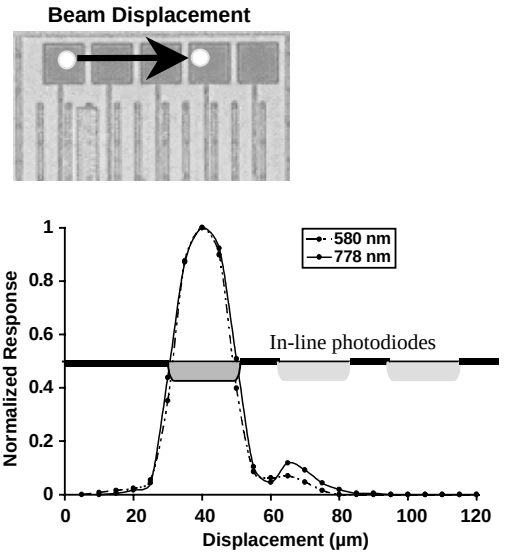

Fig. 14. Spotscan analysis of in-line photodiodes (side dimension 20 μm) implemented in a standard 0.5 μ CMOS process demonstrating the crosstalk due to diffusion mechanism.

make use of low-doped deep epitaxial layers where charge generation and collection occur and the large voltage drive (10–15 V) resulting in electric field action in regions extending up to 7–10 μ in the substrate. This allows direct collection of charges even for the near IR region and high collection efficiency. In contrast, CMOS process is made of a thin epi-layer on low resistivity substrate and uses a low voltage drive (3.3 or 5 V) giving an electric field action extending only to a few microns in the silicon depth (2–3 μm); consequently, charges will have to diffuse to be collected resulting in lower collection efficiency. This explains the drop in QE starting from 700 nm. Additionally, crosstalk between detector elements (loss in resolution) increases with the wavelength (Fig. 14).

4. Status of CCD technology and features

CCD technology is now very mature and it provides a set of very nice performances such as high Quantum Efficiency (QE), low readout noise (10–15 e^- rms at 10 MHz, a few electrons for low scan), very low Dark Current (in the typical range of 10–20 pA/cm^2), high dynamic range (typically

75 dB for Front Illumination and 90 dB for Backside Illumination). It offers very large-size arrays in terms of both pixel number (6 Mpix, 16 Mpix, …, 63 Mpix with minimum pixel pitch ranging from 5 to 9 μm), and area (up to 40×55 mm or even a full 6″ wafer size). CCD manufacturers have been continuously very innovative since the invention of concepts to circumvent the key difficulties and to improve the performances: buried channel adoption to improve the charge transfer efficiency, anti-blooming devices (often at the expense of reduced Fill-Factor), inverted (Multi Phase Pinned) mode to reduce the DC, reduction of phase number, use of open-gate or thinning plus backside illumination associated with antireflective (AR) coating to improve QE, development of UV conversion layers to extend the response in the UV region or high resistivity devices (deep depletion CCD) for X-rays detection. However, it should be noted that only a very limited set of manufacturers in the world has the capability of producing the ultimate performances backside illuminated thinned CCDs. Recent advances have focused on reduction of noise by increasing the sensitivity up to 15 μV/e by minimization of C_{fd} and QE improvements of frontside illuminated CCDs through the use of transparent gate material such as Indium Tin Oxide (ITO) [18] that have been associated recently with micro-lenses that focus the photon flux on the transparent gate [19]. Fig. 15 shows the QE data for several CCD technologies and demonstrates the strong improvement obtained by this technique. The use of charge multiplication by impact ionization in an additional section of output register driven by higher clock value (up to 40 V) [20] allows one to address very low light conditions requirements without the use of intensifier.

Despite this impressive amount of progress, CCD still suffers from several drawbacks, most of them related to CCD architecture (Fig. 1): serial access to image being slow for large-size arrays, high power dissipation (as CV^2f) due to intrinsic capacitive nature of gates and the use of large voltage drive levels for vertical and horizontal clocks that allow for efficient charge transfer, lack of random access and windowing capability. Some others are related to the technology itself that do not allow, due to the lack of powerful

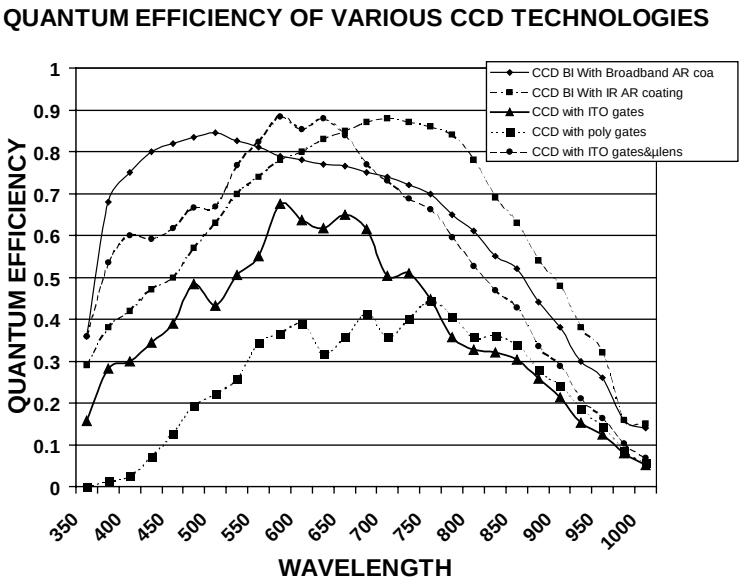

Fig. 15. Comparison of QE for various CCD technologies: Backside illuminated (EEV 30-11 BI) with broadband AR coating and with IR AR coating, traditional poly-gates (Kodak KAF 1400), ITO gates (Kodak KAF 1401E), ITO gates with micro-lenses (Kodak from Ref. [19]).

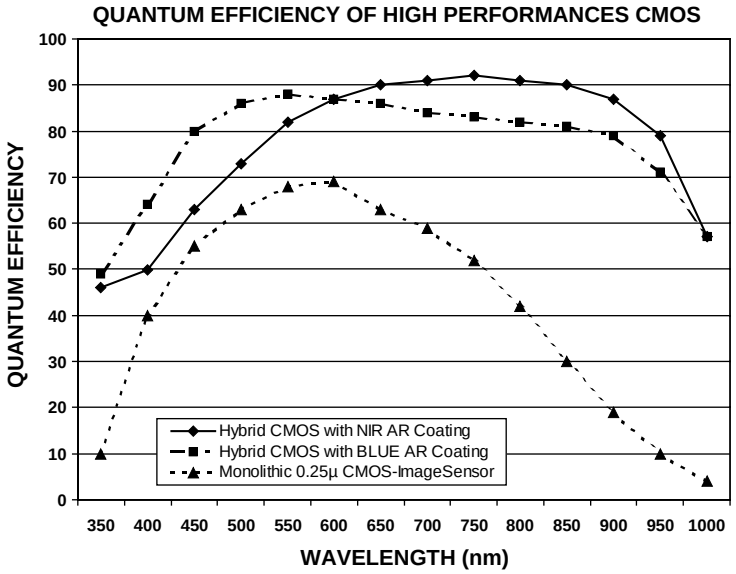

Fig. 16. Comparison of QE for high performance CMOS detectors from Rockwell Scientific: monolithic 0.25 μ CMOS process (PROCAM product) and hybrid CMOS detectors (HiViSI product) with NIR AR coating and Blue AR coating.

complementary devices, for easy integration of peripheral functions and that prevent, because of its proprietary nature, the customers to have second sources.

5. Perspectives of CMOS detectors improvements

Standard CMOS process offers few ways of managing performance trade-off at the design level but essential improvements related to QE require optimizations at the process level: optimization of photodetector doping profile to improve photocharge collection and top layers to enhance optical transmission. Thanks to new high volume markets such as Digital Still Photography or Cellphone cameras, several silicon founders have invested in the development of additional process module (CMOS Image Sensors—CIS process) to add optimized photodiodes on the top of existing mixed signal process, targeting high QE and low DC ($<100\,pA/cm^2$). Starting only a few years ago with 0.5 μ generation, this approach have been applied successfully to the 0.35 and 0.25 μ generations available nowadays and very soon will be applied for the 0.18 μ generation, and this will allow the CMOS to compete with CCD very efficiently, providing Dynamic Range up to 70 dB. As an example, Fig. 16 shows the QE of a recent image sensor for HDTV (PROCAM product) from Rockwell Scientific manufactured with a 0.25 μ CIS process (5 μm × 5 μm pixel with microlenses) [5,21] that demonstrate an impressive improvement (QE peak at 70%) when compared to standard process, while keeping other CMOS advantages. Taking advantage of the large amount of work that have been done in the CCD domain, several techniques are applied to CMOS: microlenses are widely used to compensate the loss of Fill-Factor, backside thinning is currently being investigated [22], and the use of fully depleted (“pinned”) photodiode [23,24] allows the implementation of a complete charge transfer mode in the said 4T or “low noise pixel” configuration (Fig. 17) in a manner very similar to the photogate one thus offering high conversion gain and low noise (elimination of KTC noise through CDS readout). Additionally, QE is improved in the blue region and DC is reduced. This type of photodiode has been adopted by several manufacturers and is

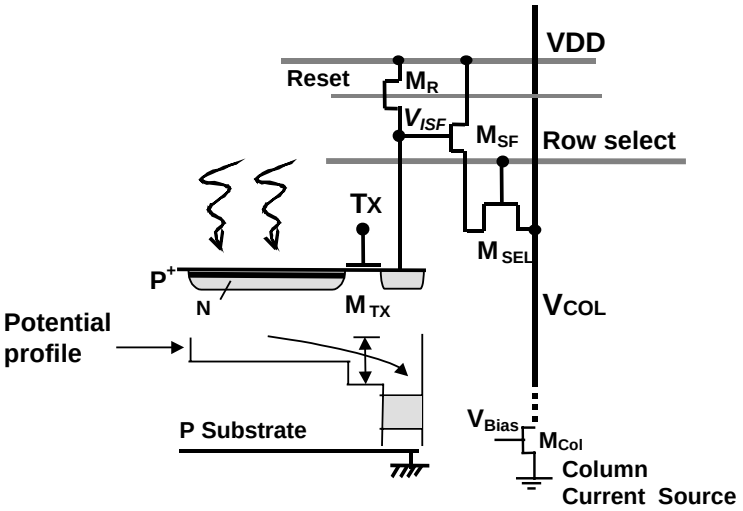

Fig. 17. Pinned photodiode configuration (charge transfer mode to low-capacitance node through TX transistor).

presently one of the best candidate for low noise detection [25].

Several attempts departing from the monolithic approach, but keeping CMOS architectural advantages, are on the way to get both near-100% Fill-Factor and efficient charge collection, being based on hybridization of photodiodes made in an optimized detection layer on the top of a CMOS readout circuit. In one approach, called Thin Film on ASIC (TFA)[25], a P-I-N a-Si:H detection layer covered by transparent front contact (ZnO for example) and aluminum rear electrode is deposited on a readout circuit thus allowing P-I-N photodiode to be realized with 100% Fill-Factor; it provides peak QE of 80% at 550 nm but due to the band gap of a-Si:H (1.78 eV) the response range is limited to 750 nm. In a second approach derived from hybrid Infrared Detectors (Fig. 18), AR coated photodiodes made of crystalline Si are hybridized to a CMOS readout circuit (that includes SF of CTIA) using indium bumps [26]; products from Rockwell Scientific HyViSI or Raytheon Aladdin [27] use this approach to provide, thanks to use of dedicated AR coating, backside illuminated thinned-CCD performance level for the visible and NIR spectral range. Fig. 16 shows, as an example, the QE curves of the Rockwell Scientific HyViSI. It should be noticed that this approach allows for a very large commonality with IR detector regarding the readout aspects (readout modes, noise, power dissipation).

6. Conclusions

CCD technology, due to process specialization, has been able to provide top-level performances for detection but at the cost of both several drawbacks for the user and, for the best products thinned and backside illuminated, the risk associated with the very limited number of procurement sources. It remains the first-choice technology for very high-end applications. On the other hand, CMOS detectors have intrinsic advantages (low power consumption, readout rate, noise, radiation hardness, integration capability) that make them well suited for several applications. Thanks to recent efforts for developing optimized detectors compatible with CMOS core process, CMOS can provide enhanced QE and DC (although it remains weaker than CCD for that aspect). New approach based on hybrid organization has the ambition of reaching the best CCD performance level in a close synergy with IR detectors and will certainly

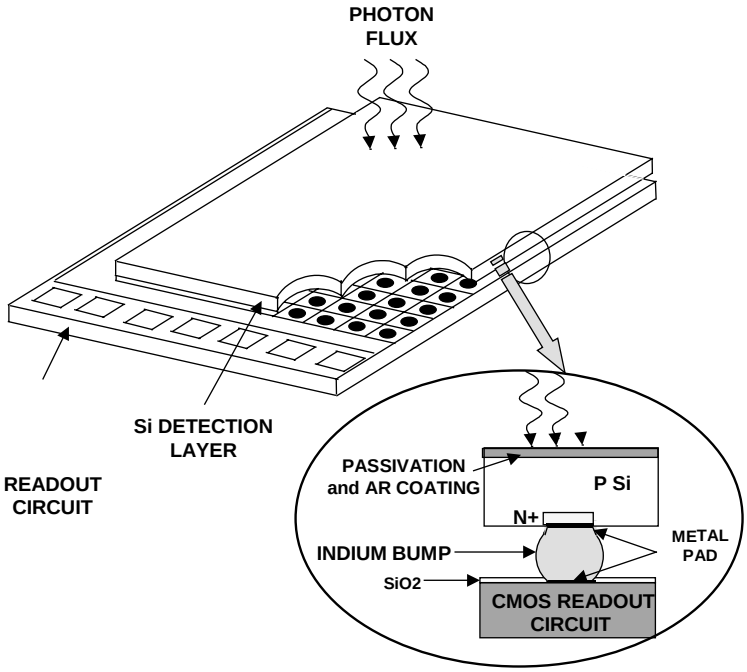

Fig. 18. Organization of CMOS hybrid detectors.

push CCD technology farther to get ultimate performances.

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