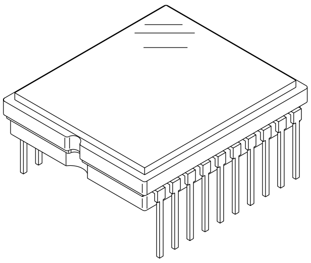
SONY

ICX411AQ

Diagonal 8.98mm (Type 1/1.8) Frame Readout CCD Image Sensor with a Square Pixel for Color Cameras


20 pin DIP (Plastic)

Description

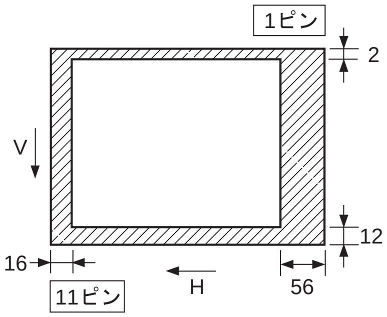
The ICX411AQ is a diagonal 8.98mm (Type 1/1.8) interline CCD solid-state image sensor with a square pixel array and 3.98M effective pixels. Frame readout allows all pixels' signals to be output independently within approximately 1/4.28 second.

Also, number of vertical pixels decimation allows output of 30 frames per second in high frame rate readout mode.

This chip features an electronic shutter with variable charge-storage time.

R, G, B primary color mosaic filters are used as the color filters, and at the same time high sensitivity and low dark current are achieved through the adoption of Super HAD CCD technology.

This chip is suitable for applications such as electronic still cameras, etc.



Optical black position
(Top View)

Features
- Supports frame readout
- High horizontal and vertical resolution
- Supports high frame rate readout mode: 30 frames/s, 25 frames/s,
  AF1 mode: 60 frames/s, 50 frames/s,
  AF2 mode: 120 frames/s, 100 frames/s
- Square pixel
- Horizontal drive frequency: 24MHz
- No voltage adjustments (reset gate and substrate bias are not adjusted.)
- R, G, B primary color mosaic filters on chip
- High sensitivity, low dark current
- Continuous variable-speed shutter
- Excellent anti-blooming characteristics
- Exit pupil distance recommended range –20 to –100mm
- 20-pin high-precision plastic package

Device Structure
- Interline CCD image sensor
- Total number of pixels: 2384 (H) × 1734 (V) approx. 4.13M pixels
- Number of effective pixels: 2312 (H) × 1720 (V) approx. 3.98M pixels
- Number of active pixels: 2308 (H) × 1712 (V) approx. 3.95M pixels diagonal 8.980mm
- Number of recommended recording pixels:
  2272 (H) × 1704 (V) approx. 3.87M pixels diagonal 8.875mm aspect ratio 4:3
- Chip size: 8.1mm (H) × 6.6mm (V)
- Unit cell size: 3.125µm (H) × 3.125µm (V)
- Optical black: Horizontal (H) direction: Front 16 pixels, rear 56 pixels
  Vertical (V) direction: Front 12 pixels, rear 2 pixels
- Number of dummy bits: Horizontal 28
  Vertical 1 (even fields only)
- Substrate material: Silicon

Super **HAD CCD** TM

* Super HAD CCD is a trademark of Sony Corporation. The Super HAD CCD is a version of Sony's high performance CCD HAD (Hole-Accumulation Diode) sensor with sharply improved sensitivity by the incorporation of a new semiconductor technology developed by Sony Corporation.

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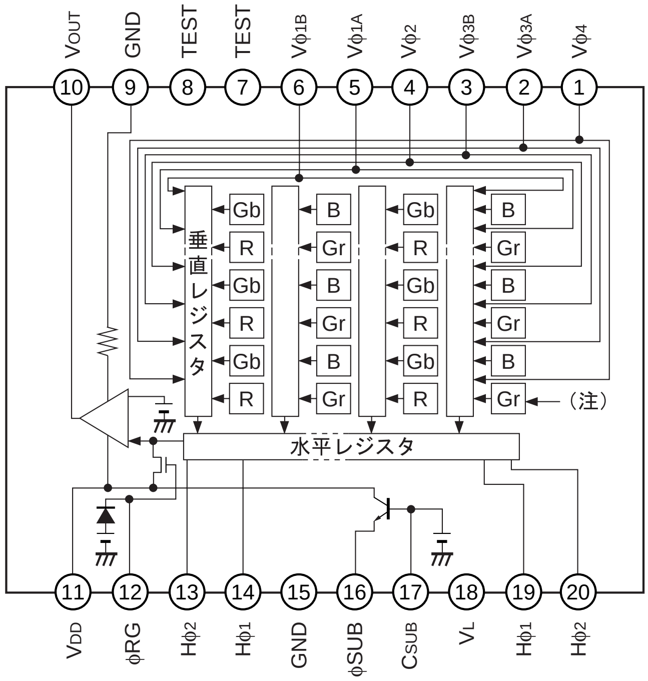
Block Diagram and Pin Configuration

(Top View)


V_{OUT}
GND
TEST
TEST
$V\phi_{1B}$
$V\phi_{1A}$
$V\phi_{2}$
$V\phi_{3B}$
$V\phi_{3A}$
$V\phi_{4}$
10
9
8
7
6
5
4
3
2
1
垂直レジスタ
Gb
R
B
Gr
（注）
水平レジスタ
11
12
13
14
15
16
17
18
19
20
V_{DD}
ϕRG
$H\phi_{2}$
$H\phi_{1}$
GND
ϕSUB
C_{SUB}
V_L
$H\phi_{1}$
$H\phi_{2}$

（注）□：フォトセンサ

Pin Description

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	$V\phi_{4}$	Vertical register transfer clock	11	V_{DD}	Supply voltage
2	$V\phi_{3A}$	Vertical register transfer clock	12	ϕRG	Reset gate clock
3	$V\phi_{3B}$	Vertical register transfer clock	13	$H\phi_{2}$	Horizontal register transfer clock
4	$V\phi_{2}$	Vertical register transfer clock	14	$H\phi_{1}$	Horizontal register transfer clock
5	$V\phi_{1A}$	Vertical register transfer clock	15	GND	GND
6	$V\phi_{1B}$	Vertical register transfer clock	16	ϕSUB	Substrate clock
7	TEST	Test pin[*1]	17	C_{SUB}	Substrate bias[*2]
8	TEST	Test pin[*1]	18	V_L	Protective transistor bias
9	GND	GND	19	$H\phi_{1}$	Horizontal register transfer clock
10	V_{OUT}	Signal output	20	$H\phi_{2}$	Horizontal register transfer clock

[*1] Leave this pin open

[*2] DC bias is generated within the CCD, so that this pin should be grounded externally through a capacitance of 0.1µF.

Absolute Maximum Ratings

Item		Ratings	Unit	Remarks
Against ϕSUB	V_{DD}, V_{OUT}, ϕRG – ϕSUB	–40 to +12	V	
	$V\phi_{1A}$, $V\phi_{1B}$, $V\phi_{3A}$, $V\phi_{3B}$ – ϕSUB	–50 to +15	V	
	$V\phi_{2}$, $V\phi_{4}$, V_{L} – ϕSUB	–50 to +0.3	V	
	$H\phi_{1}$, $H\phi_{2}$, GND – ϕSUB	–40 to +0.3	V	
	C_{SUB} – ϕSUB	–25 to	V	
Against ϕGND	V_{DD}, V_{OUT}, ϕRG, C_{SUB} – GND	–0.3 to +22	V	
	$V\phi_{1A}$, $V\phi_{1B}$, $V\phi_{2}$, $V\phi_{3A}$, $V\phi_{3B}$, $V\phi_{4}$ – GND	–10 to +18	V	
	$H\phi_{1}$, $H\phi_{2}$ – GND	–10 to +6.5	V	
Against ϕV_{L}	$V\phi_{1A}$, $V\phi_{1B}$, $V\phi_{3A}$, $V\phi_{3B}$ – V_{L}	–0.3 to +28	V	
	$V\phi_{2}$, $V\phi_{4}$, $H\phi_{1}$, $H\phi_{2}$, GND – V_{L}	–0.3 to +15	V	
Between input clock pins	Voltage difference between vertical clock input pins	to +15	V	[*1]
	$H\phi_{1}$ – $H\phi_{2}$	–6.5 to +6.5	V	
	$H\phi_{1}$, $H\phi_{2}$ – $V\phi_{4}$	–10 to +16	V	
Storage temperature		–30 to +80	°C	
Guaranteed temperature of performance		–10 to +60	°C	
Operating temperature		–10 to +75	°C	

[*1] +24V (Max.) when clock width < 10µs, clock duty factor < 0.1%.
+16V (Max.) is guaranteed for turning on or off power supply.

Bias Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage	V_{DD}	14.55	15.0	15.45	V	
Protective transistor bias	V_{L}	*1				
Substrate clock	ϕSUB	*2				
Reset gate clock	ϕRG	*2				

*1 V_{L} setting is the V_{VL} voltage of the vertical clock waveform, or the same voltage as the V_{L} power supply for the V driver should be used.

*2 Do not apply a DC bias to the substrate clock and reset gate clock pins, because a DC bias is generated within the CCD.

DC Characteristics

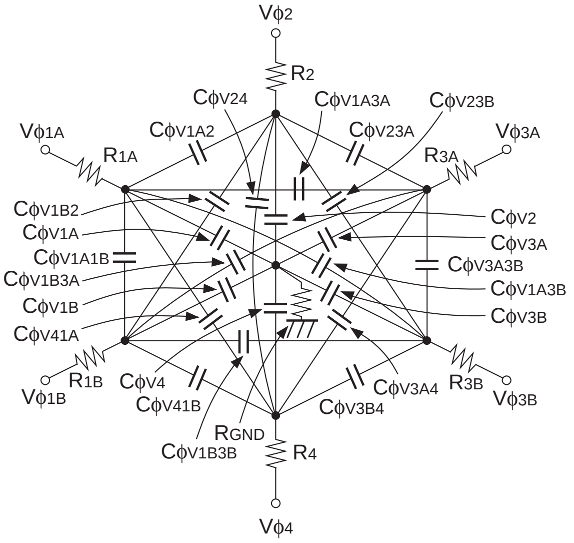
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply current	I_{DD}	3.0	7.0	10.0	mA	

Clock Voltage Conditions

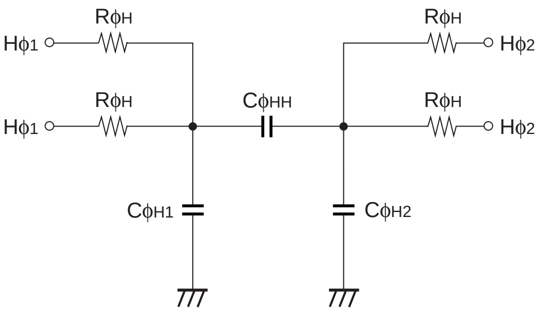
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform Diagram	Remarks
Readout clock voltage	V_{VT}	14.55	15.0	15.45	V	1	
Vertical transfer clock voltage	V_{VH1}, V_{VH2}	–0.05	0	0.05	V	2	$V_{VH} = (V_{VH1} + V_{VH2})/2$
	V_{VH3}, V_{VH4}	–0.2	0	0.05	V	2	
	V_{VL1}, V_{VL2}, V_{VL3}, V_{VL4}	–8.0	–7.5	–7.0	V	2	$V_{VL} = (V_{VL3} + V_{VL4})/2$
	$V_{\phi V}$	6.8	7.5	8.05	V	2	$V_{\phi V} = V_{VHn} – V_{VLn}$ (n = 1 to 4)
	$V_{VH3} – V_{VH}$	–0.25		0.1	V	2	
	$V_{VH4} – V_{VH}$	–0.25		0.1	V	2	
	V_{VHH}			0.9	V	2	High-level coupling
	V_{VHL}			0.9	V	2	High-level coupling
	V_{VLH}			0.9	V	2	Low-level coupling
	V_{VLL}			0.7	V	2	Low-level coupling
Horizontal transfer clock voltage	$V_{\phi H}$	4.75	5.0	5.25	V	3	
	V_{HL}	–0.05	0	0.05	V	3	
	V_{CR}	0.8	2.5		V	3	Cross-point voltage
Reset gate clock voltage	$V_{\phi RG}$	3.0	3.3	5.25	V	4	
	$V_{RGLH} – V_{RGLL}$			0.4	V	4	Low-level coupling
	$V_{RGL} – V_{RGLm}$			0.5	V	4	Low-level coupling
Substrate clock voltage	$V_{\phi SUB}$	21.5	22.5	23.5	V	5	

Clock Equivalent Circuit Constants

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C\phi_{V1A}$, $C\phi_{V3A}$		1200		pF	
	$C\phi_{V1B}$, $C\phi_{V3B}$		4700		pF	
	$C\phi_{V2}$, $C\phi_{V4}$		3300		pF	
Capacitance between vertical transfer clocks	$C\phi_{V1A2}$, $C\phi_{V3A4}$		470		pF	
	$C\phi_{V1B2}$, $C\phi_{V3B4}$		560		pF	
	$C\phi_{V23A}$, $C\phi_{V41A}$		150		pF	
	$C\phi_{V23B}$, $C\phi_{V41B}$		220		pF	
	$C\phi_{V1A3A}$		39		pF	
	$C\phi_{V1B3B}$		220		pF	
	$C\phi_{V1A3B}$, $C\phi_{V1B3A}$		56		pF	
	$C\phi_{V24}$		82		pF	
	$C\phi_{V1A1B}$, $C\phi_{V3A3B}$		68		pF	
Capacitance between horizontal transfer clock and GND	$C\phi_{H1}$, $C\phi_{H2}$		33		pF	
Capacitance between horizontal transfer clocks	$C\phi_{HH}$		82		pF	
Capacitance between reset gate clock and GND	$C\phi_{RG}$		8		pF	
Capacitance between substrate clock and GND	$C\phi_{SUB}$		1000		pF	
Vertical transfer clock series resistor	R_{1A}, R_{1B}, R_2, R_{3A}, R_{3B}, R_4		62		Ω	
Vertical transfer clock ground resistor	R_{GND}		18		Ω	
Horizontal transfer clock series resistor	$R\phi_H$		12		Ω	


Vφ2
R2
CφV24
CφV1A3A
CφV23B
Vφ1A
CφV1A2
CφV23A
Vφ3A
R1A
R3A
CφV1B2
CφV1A
CφV1A1B
CφV1B3A
CφV1B
CφV41A
CφV2
CφV3A
CφV3A3B
CφV1A3B
CφV3B
R1B
CφV4
Vφ1B
CφV41B
CφV3A4
R3B
Vφ3B
CφV3B4
RGND
CφV1B3B
R4
Vφ4

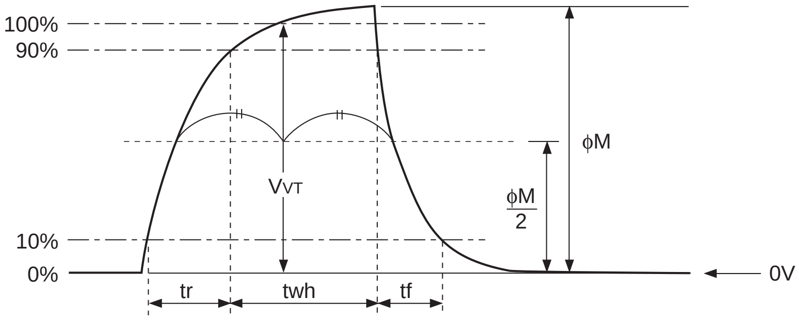
Vertical transfer clock equivalent circuit


RφH
Hφ1
RφH
Hφ1
CφHH
RφH
Hφ2
RφH
Hφ2
CφH1
CφH2

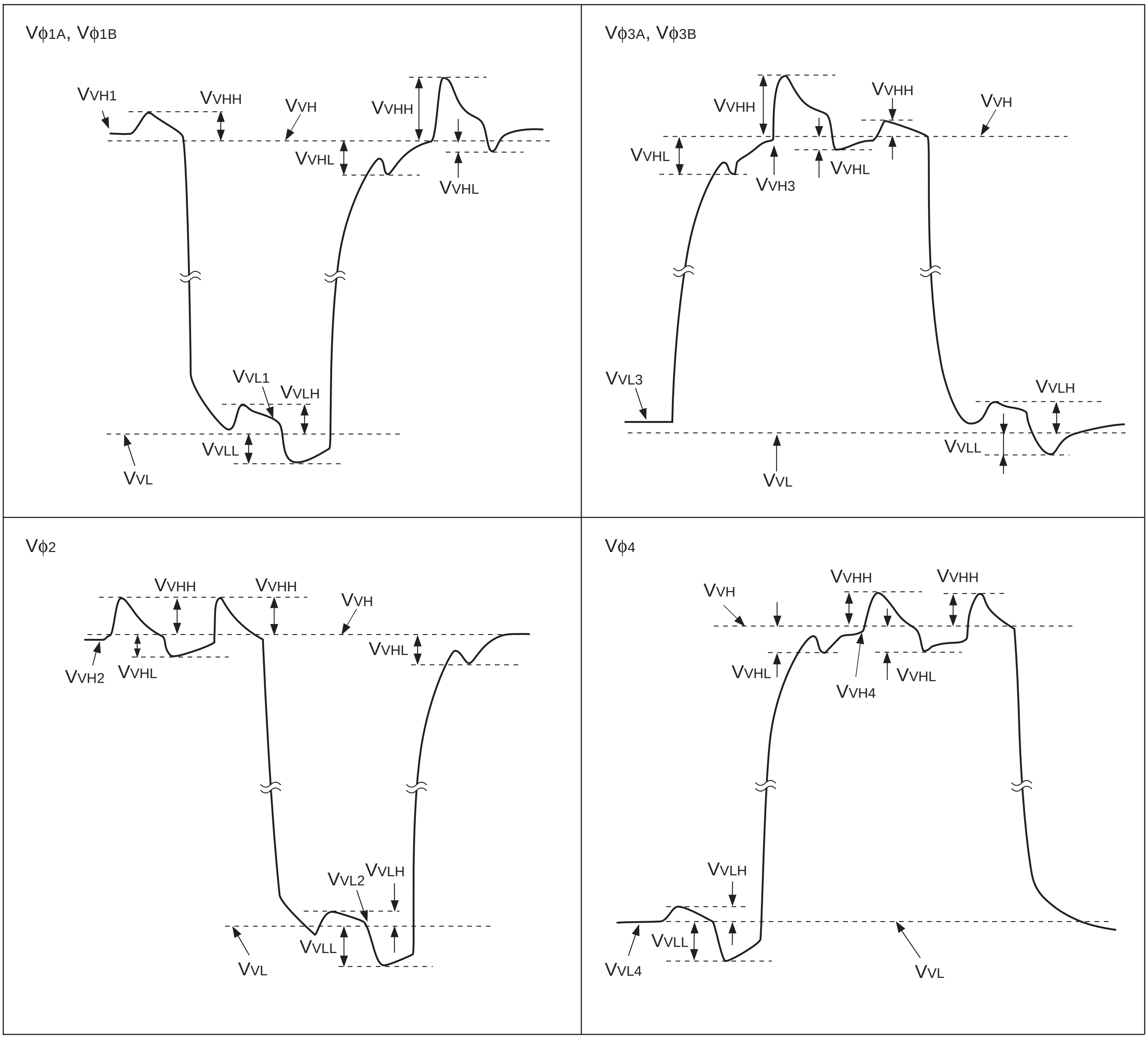
Horizontal transfer clock equivalent circuit

Drive Clock Waveform Conditions

(1) Readout clock waveform


100%
90%
10%
0%
VVT
φM
φM/2
0V
tr
twh
tf

(2) Vertical transfer clock waveform

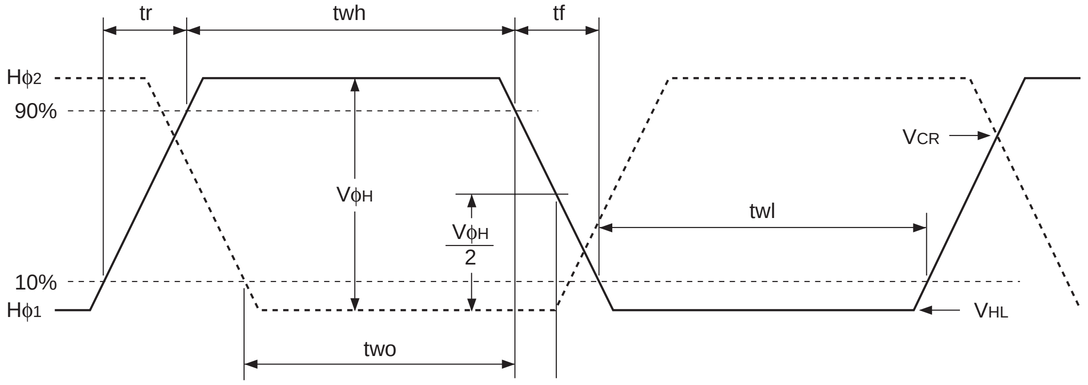

Vφ1A, Vφ1B
VVH1
VVHH
VVH
VVHH
VVHL
VVHL
VVL1
VVLH
VVLL
VVL
Vφ3A, Vφ3B
VVHH
VVHH
VVH
VVHL
VVH3
VVHL
VVL3
VVLH
VVLL
VVL
Vφ2
VVHH
VVHH
VVH
VVHL
VVH2
VVHL
VVL2
VVLH
VVLL
VVL
Vφ4
VVHH
VVHH
VVH
VVHL
VVH4
VVHL
VVLH
VVLL
VVL4
VVL

$V_{VH} = (V_{VH1} + V_{VH2})/2$

$V_{VL} = (V_{VL3} + V_{VL4})/2$

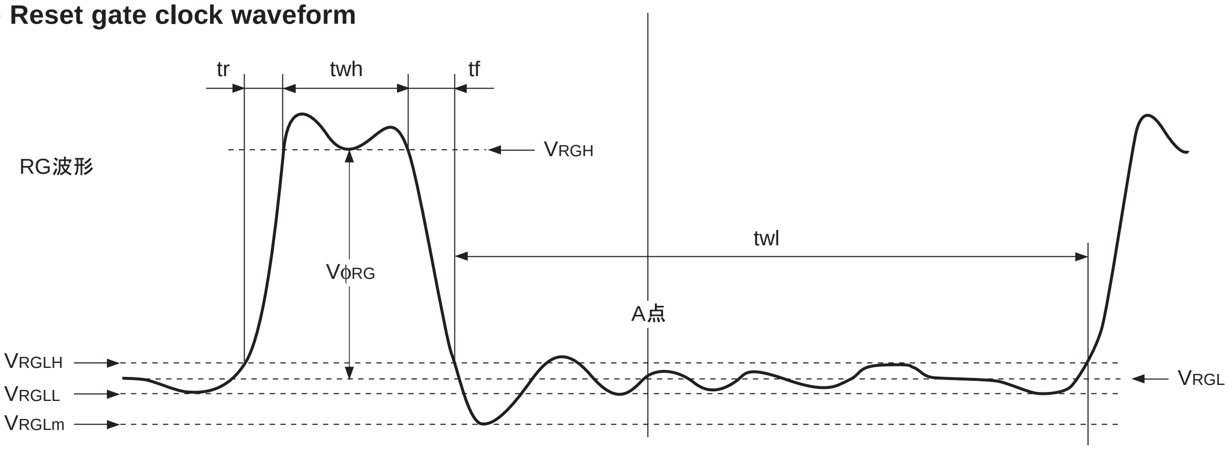
$V_{\phi V} = V_{VH}n - V_{VL}n$ (n = 1 to 4)

(3) Horizontal transfer clock waveform


tr
twh
tf
Hϕ2
90%
VϕH
VϕH/2
VCR
twl
10%
Hϕ1
VHL
two

Cross-point voltage for the $H\phi_1$ rising side of the horizontal transfer clocks $H\phi_1$ and $H\phi_2$ waveforms is V_{CR}.
The overlap period for twh and twl of horizontal transfer clocks $H\phi_1$ and $H\phi_2$ is two.

(4) Reset gate clock waveform


tr
twh
tf
RG波形
VRGH
VϕRG
twl
A点
VRGLH
VRGLL
VRGLm
VRGL

V_{RGLH} is the maximum value and V_{RGLL} is the minimum value of the coupling waveform during the period from Point A in the above diagram until the rising edge of RG.
In addition, V_{RGL} is the average value of V_{RGLH} and V_{RGLL}.

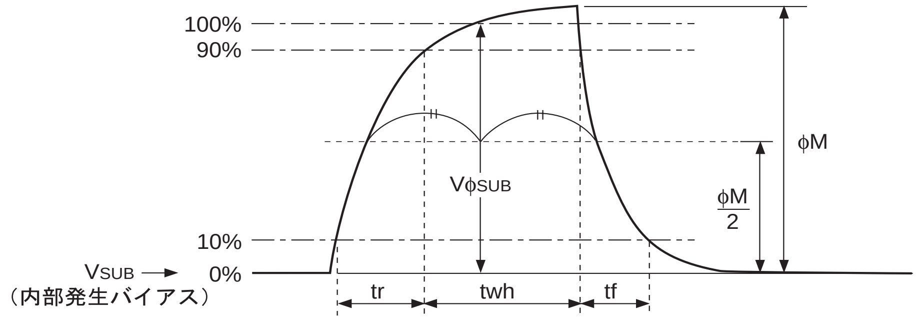
$$V_{RGL} = (V_{RGLH} + V_{RGLL})/2$$

Assuming V_{RGH} is the minimum value during the interval with twh, then:

$$V\phi_{RG} = V_{RGH} - V_{RGL}$$

Negative overshoot level during the falling edge of RG is V_{RGLm}.

(5) Substrate clock waveform


100%
90%
ϕM
VϕSUB
ϕM/2
10%
VSUB
（内部発生バイアス）
0%
tr
twh
tf

Clock Switching Characteristics (Horizontal drive frequency: 24MHz)

Item	Symbol	twh			twl			tr			tf			Unit	Remarks
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Readout clock	V_T	3.10	3.33						0.5			0.5		μs	During readout
Vertical transfer clock	$V\phi_{1A}$, $V\phi_{1B}$, $V\phi_2$, $V\phi_{3A}$, $V\phi_{3B}$, $V\phi_4$										15		250	ns	When using CXD3400N
Horizontal transfer clock	$H\phi_1$	10.5	14.6		10.5	14.6			6.4	10.5		6.4	10.5	ns	tf ≥ tr – 2ns
	$H\phi_2$	10.5	14.6		10.5	14.6			6.4	10.5		6.4	10.5		
Reset gate clock	ϕRG	6	8			37			4			3		ns	
Substrate clock	ϕSUB	1.6	2.7							0.5			0.5	μs	During drain charge

Item	Symbol	two			Unit	Remarks
		Min.	Typ.	Max.		
Horizontal transfer clock	$H\phi_1$, $H\phi_2$	10.5	14.6		ns	

Spectral Sensitivity Characteristics (excludes lens characteristics and light source characteristics)

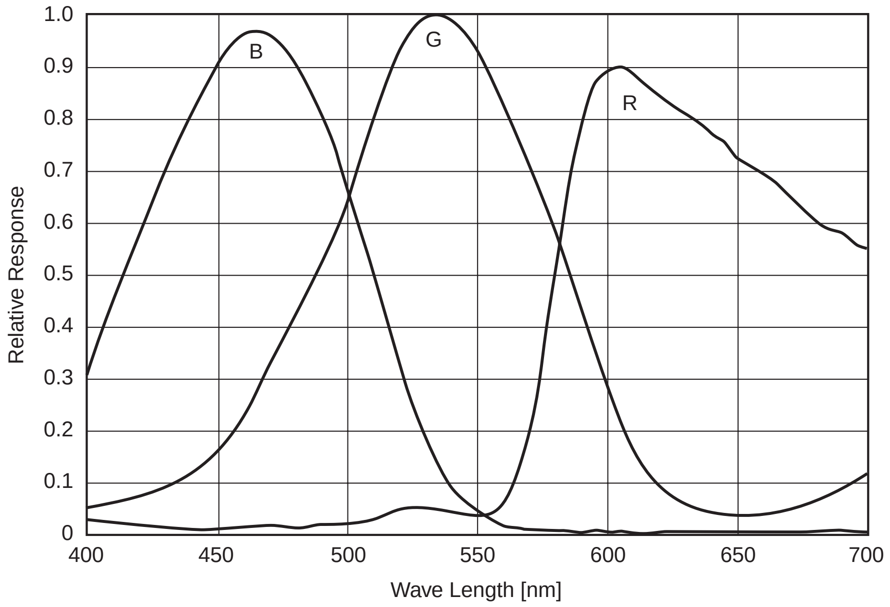


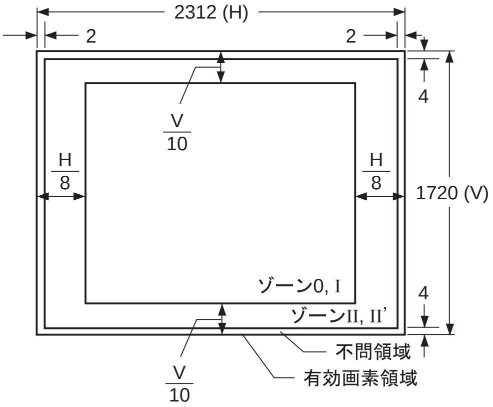
Image Sensor Characteristics (horizontal drive frequency: 24MHz) (Ta = 25°C)

Item		Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks
G Sensitivity		Sg	180	220	285	mV	1	1/30s accumulation
Sensitivity comparison	R	Rr	0.35	0.50	0.65		1	
	B	Rb	0.40	0.55	0.70		1	
Saturation signal		Vsat	380			mV	2	Ta = 60°C
Smear		Sm		–90	–81.2	dB	3	Frame readout mode*1
				–79	–70.1			High frame rate readout mode
Video signal shading		SHg			20	%	4	Zone 0 and I
					25			Zone 0 to II'
Dark signal		Vdt			12	mV	5	Ta = 60°C, 4.28 frame/s
Dark signal shading		ΔVdt			6	mV	6	Ta = 60°C, 4.28 frame/s, *2
Line crawl G		Lcg			3.8	%	7	
Line crawl R		Lcr			3.8	%	7	
Line crawl B		Lcb			3.8	%	7	
Lag		Lag			0.5	%	8	

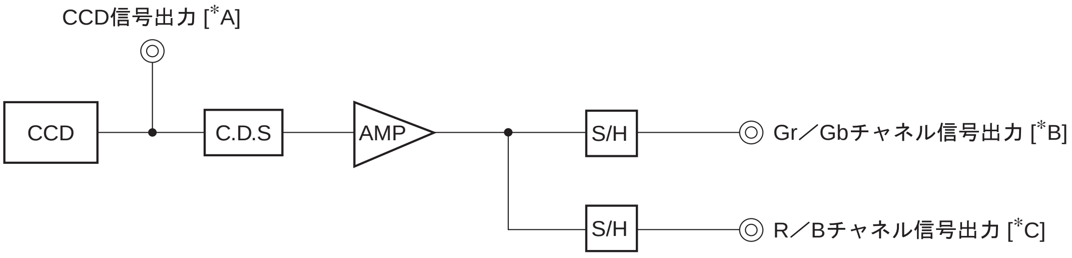
*1 After closing the mechanical shutter, the smear can be reduced to below the detection limit by performing vertical register sweep operation.

*2 Excludes vertical dark signal shading caused by vertical register high-speed transfer.

Zone Definition of Video Signal Shading


2312 (H)
2
2
4
1720 (V)
4
V/10
H/8
H/8
ゾーン0, I
ゾーンII, II'
V/10
不問領域
有効画素領域

Measurement System


CCD信号出力 [*A]
CCD
C.D.S
AMP
S/H
S/H
Gr／Gbチャネル信号出力 [*B]
R／Bチャネル信号出力 [*C]

Note) Adjust the amplifier gain so that the gain between [*A] and [*B], and between [*A] and [*C] equals 1.

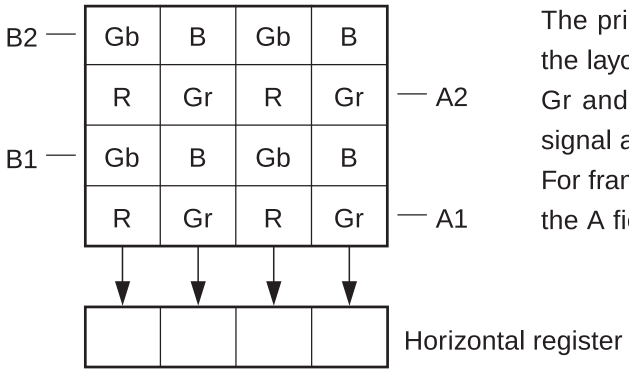
Image Sensor Characteristics Measurement Method

◎ Measurement conditions

(1) In the following measurements, the device drive conditions are at the typical values of the bias and clock voltage conditions, and the frame readout mode is used.

(2) In the following measurements, spot blemishes are excluded and, unless otherwise specified, the optical black level (OB) is used as the reference for the signal output, which is taken as the value of the Gr/Gb channel signal output or the R/B channel signal output of the measurement system.

◎ Color coding of this image sensor & Readout



B2	Gb	B	Gb	B	
	R	Gr	R	Gr	A2
B1	Gb	B	Gb	B	
	R	Gr	R	Gr	A1

Color Coding Diagram

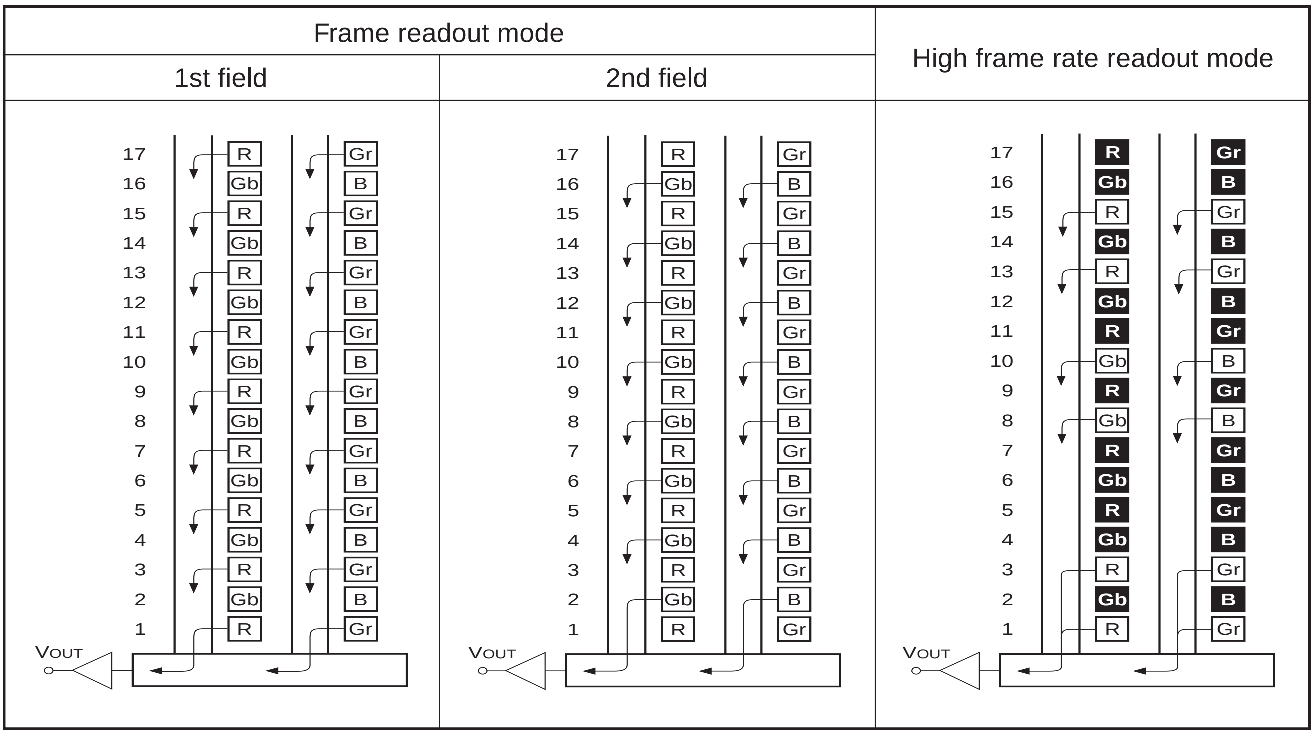
The primary color filters of this image sensor are arranged in the layout shown in the figure on the left (Bayer arrangement). Gr and Gb denote the G signals on the same line as the R signal and the B signal, respectively.
For frame readout, the A1 and A2 lines are output as signals in the A field, and the B1 and B2 lines in the B field.

◎ Readout modes

1. Readout modes list

Mode name		Frame rate	Number of effective output lines
Frame readout mode	NTSC mode	4.28 frame/s	1720 (Odd 860, Even 860)
	PAL mode	4.17 frame/s	1720 (Odd 860, Even 860)
High frame rate readout mode	NTSC mode	30 frame/s	287
	PAL mode	25 frame/s	287
AF1 mode	NTSC mode	60 frame/s	123
	PAL mode	50 frame/s	153
AF2 mode	NTSC mode	120 frame/s	41
	PAL mode	100 frame/s	55

2. Frame readout mode, high frame rate readout mode



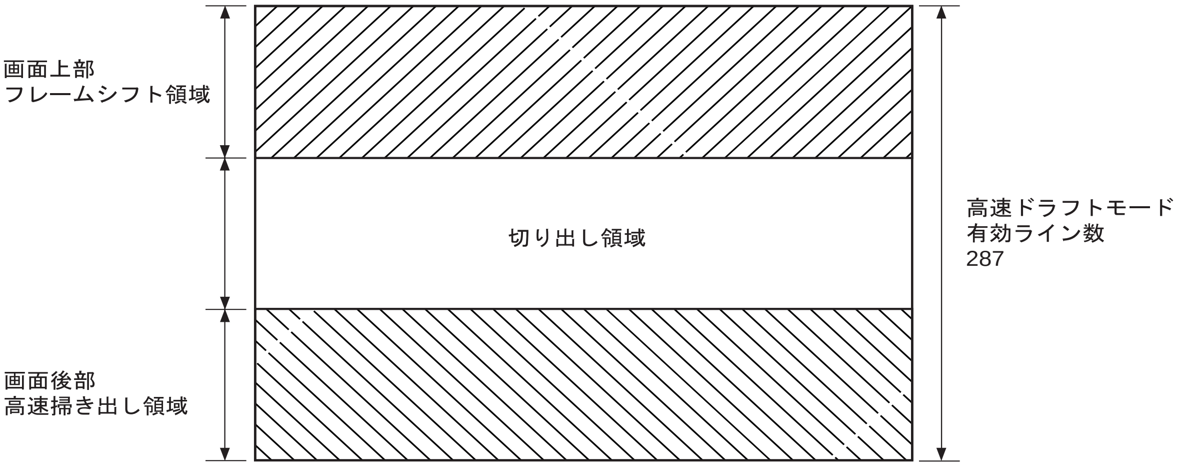
Note) Blacked out portions in the diagram indicate pixels which are not read out.

1. Frame readout mode
   In this mode, all pixel signals are divided into two fields and output.
   All pixel signals are read out independently, making this mode suitable for high resolution image capturing.

2. High frame rate readout mode
   Output is performed at 30 frames per second by reading out 4 pixels for every 12 vertical pixels and adding 2 pixels in the horizontal CCD.
   The number of output lines is 287 lines.
   This readout mode emphasizes processing speed over vertical resolution.

3. AF1 mode, AF2 mode

The AF modes increase the frame rate by cutting out a portion of the picture through high-speed elimination of the top and bottom of the picture in high frame rate readout mode. AF1 allows 1/60s and 1/50s output, and AF2 allows 1/120s and 1/100s output, so these modes are effective for raising the auto focus (AF) speed.


画面上部
フレームシフト領域
切り出し領域
画面後部
高速掃き出し領域
高速ドラフトモード
有効ライン数
287

◎ Definition of standard imaging conditions

(1) Standard imaging condition I:
Use a pattern box (luminance: 706cd/m^2, color temperature of 3200K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter and image at F5.6. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

(2) Standard imaging condition II:
Image a light source (color temperature of 3200K) with a uniformity of brightness within 2% at all angles. Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

(3) Standard imaging condition III:
Image a light source (color temperature of 3200K) with a uniformity of brightness within 2% at all angles. Use a testing standard lens (exit pupil distance –33mm) with CM500S (t = 1.0mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diagram.

1. G Sensitivity, sensitivity comparison
Set to the standard imaging condition I. After setting the electronic shutter mode with a shutter speed of 1/100s, measure the signal outputs (V_{GR}, V_{Gb}, V_R and V_B) at the center of each Gr, Gb, R and B channel screen, and substitute the values into the following formulas.

$V_G = (V_{Gr} + V_{Gb})/2$

$Sg = V_G \times \frac{100}{30}$ [mV]

$Rr = V_R/V_G$

$Rb = V_B/V_G$

2. Saturation signal
Set to the standard imaging condition II. After adjusting the luminous intensity to 20 times the intensity with the average value of the Gr signal output, 150mV, measure the minimum values of the Gr, Gb, R and B signal outputs.

3. Smear
Set to the standard imaging condition II. With the lens diaphragm at F5.6 to F8, first adjust the average value of the Gr signal output to 150mV. Measure the average values of the Gr signal output, Gb signal output, R signal output and B signal output (Gra, Gba, Ra, Ba), and then adjust the luminous intensity to 500 times the intensity with the average value of the Gr signal output, 150mV.
After the readout clock is stopped and the charge drain is executed by the electronic shutter at the respective H blankings, measure the maximum value (Vsm [mV]) independent of the Gr, Gb, R and B signal outputs, and substitute the values into the following formula.

$$Sm = 20 \times \log\left(Vsm \div \frac{Gra + Gba + Ra + Ba}{4} \times \frac{1}{500} \times \frac{1}{10}\right) \text{[dB] (1/10V method conversion value)}$$

4. Video signal shading

   Set to the standard imaging condition III. With the lens diaphragm at F5.6 to F8, adjusting the luminous intensity so that the average value of the Gr signal output is 150mV. Then measure the maximum value (Grmax [mV]) and minimum value (Grmin [mV]) of the Gr signal output and substitute the values into the following formula.

   $\text{SHg} = (\text{Grmax} - \text{Grmin})/150 \times 100\ [\%]$

5. Dark signal

   Measure the average value of the signal output (Vdt [mV]) with the device ambient temperature of 60°C and the device in the light-obstructed state, using the horizontal idle transfer level as a reference.

6. Dark signal shading

   After measuring 5, measure the maximum (Vdmax [mV]) and minimum (Vdmin [mV]) values of the dark signal output and substitute the values into the following formula.

   $\Delta\text{Vdt} = \text{Vdmax} - \text{Vdmin}\ [\text{mV}]$

7. Line crawl

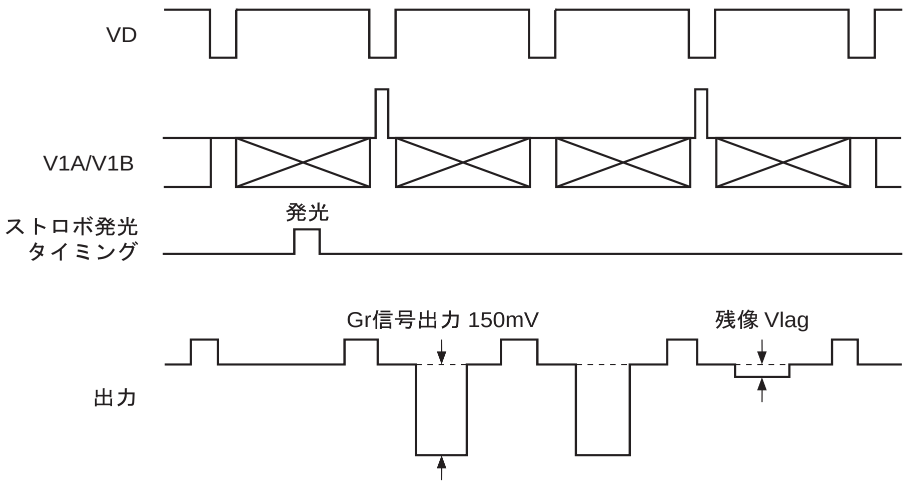
   Set to the standard imaging condition II. Adjusting the luminous intensity so that the average value of the Gr signal output is 150mV, and then insert R, G and B filters and measure the difference between G signal lines (ΔGlr, ΔGlg, ΔGlb [mV]) as well as the average value of the G signal output (Gar, Gag, Gab). Substitute the values into the following formula.

   $\text{Lci} = \dfrac{\Delta\text{Gli}}{\text{Gai}} \times 100\ [\%]\ (i = r, g, b)$

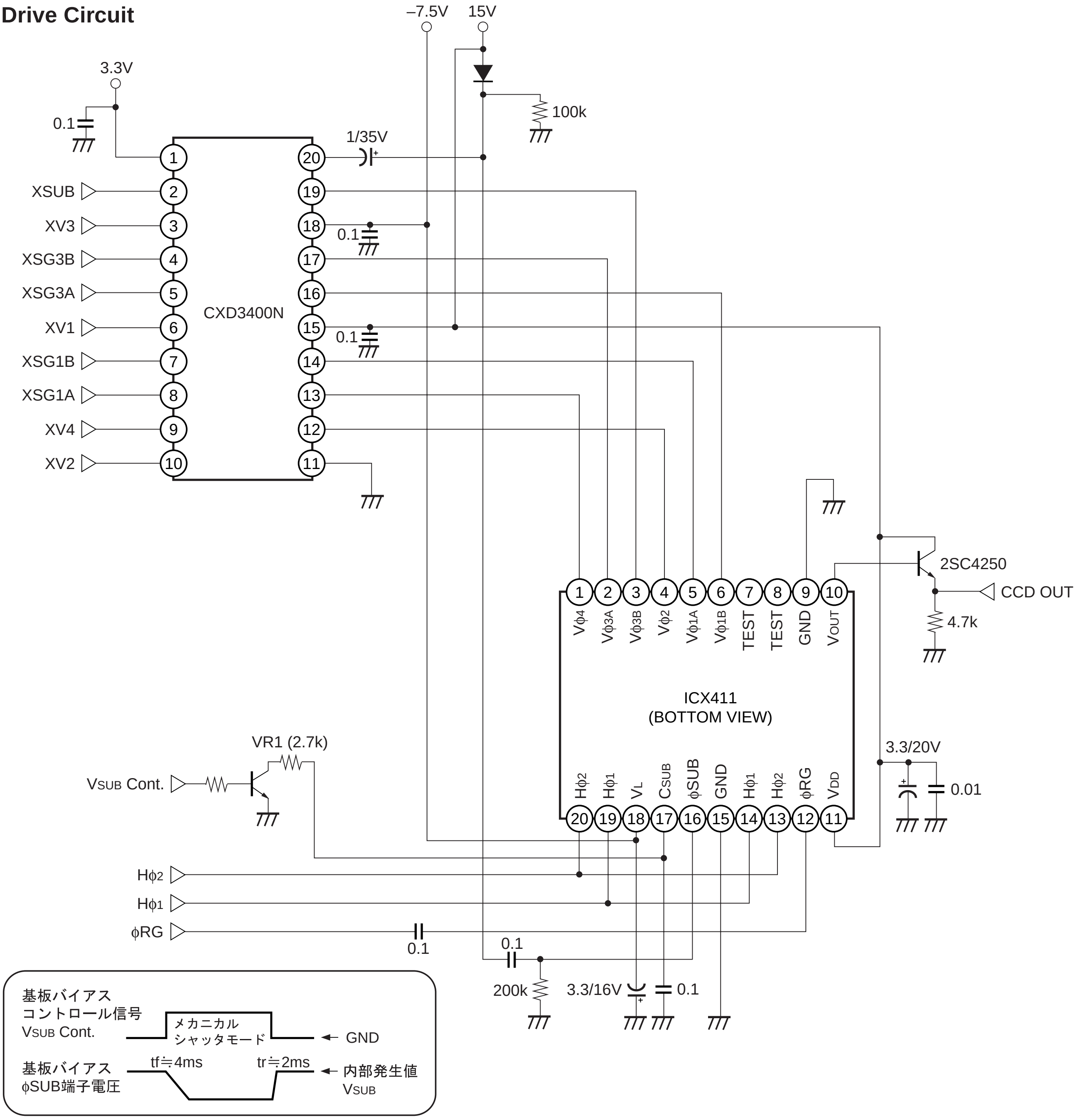
8. Lag

   Adjust the Gr signal output value generated by the strobe light to 150mV. After setting the strobe light so that it strobes with the following timing, measure the residual signal amount (Vlag). Substitute the value into the following formula.

   $\text{Lag} = (\text{Vlag}/150) \times 100\ [\%]$



Drive Circuit


–7.5V
15V
3.3V
0.1
100k
1/35V
XSUB
XV3
XSG3B
XSG3A
XV1
XSG1B
XSG1A
XV4
XV2
CXD3400N
0.1
0.1
2SC4250
CCD OUT
4.7k
Vφ4
Vφ3A
Vφ3B
Vφ2
Vφ1A
Vφ1B
TEST
TEST
GND
VOUT
ICX411
(BOTTOM VIEW)
Hφ2
Hφ1
VL
CSUB
φSUB
GND
Hφ1
Hφ2
φRG
VDD
3.3/20V
0.01
VR1 (2.7k)
VSUB Cont.
Hφ2
Hφ1
φRG
0.1
0.1
200k
3.3/16V
0.1
基板バイアス
コントロール信号
VSUB Cont.
メカニカル
シャッタモード
GND
基板バイアス
φSUB端子電圧
tf≒4ms
tr≒2ms
内部発生値
VSUB

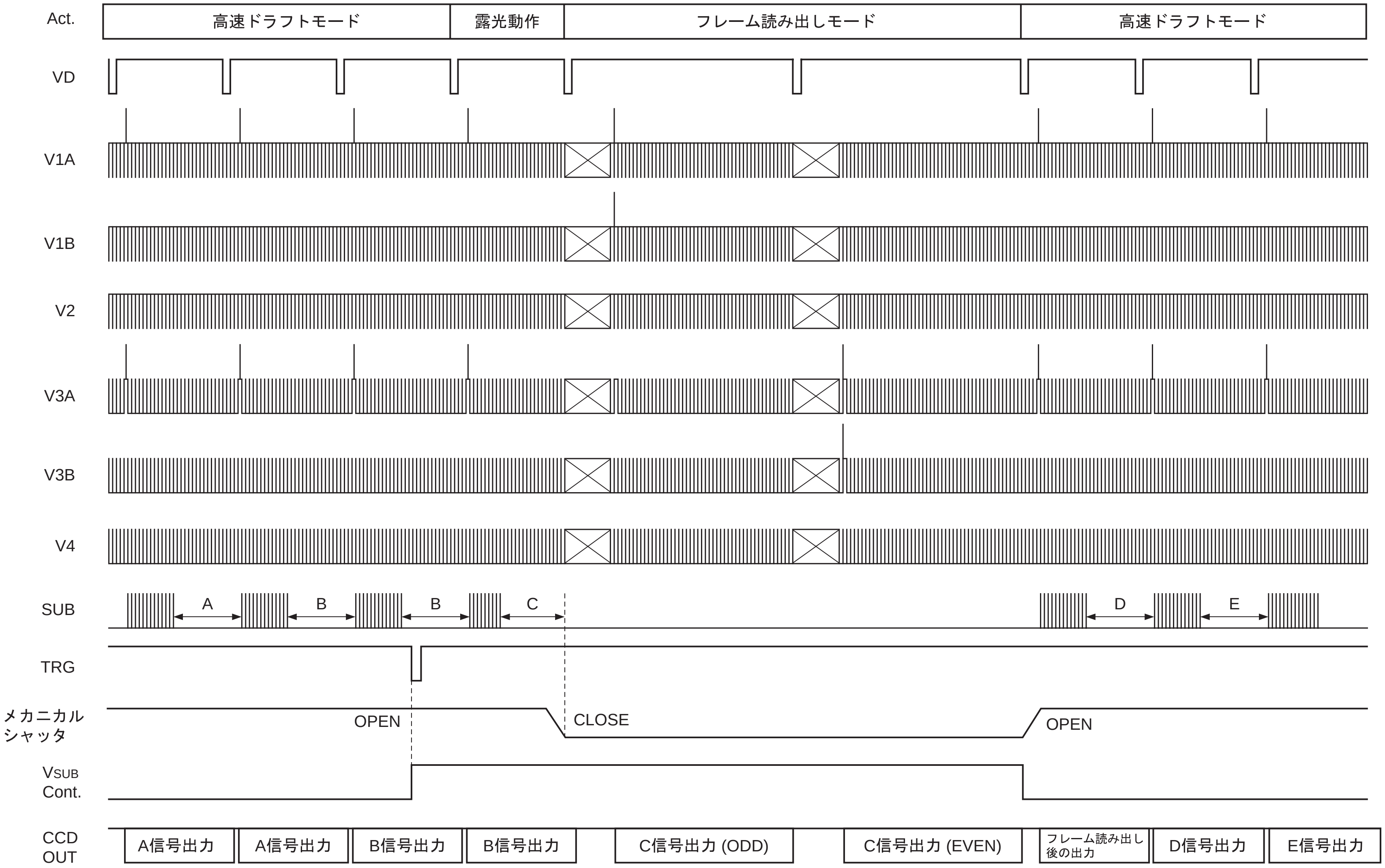
Notes) Substrate bias control

1. The saturation signal level decreases when exposure is performed using the mechanical shutter, so control the substrate bias.
2. A saturation signal level equivalent to that for continuous exposure can be assured by connecting a 2.7kΩ grounding registor to the CCD C_{SUB} pin.

Drive timing precautions

1. Blooming occurs in modes (high frame rate readout, etc.) that do not use the mechanical shutter, so do not ground the connected 2.7kΩ resistor.
2. tf is slow, so the internally generated voltage V_{SUB} may not drop to a sufficiently low level if the substrate bias control signal is not set to high level 20ms before entering the exposure period and the 2.7kΩ resistor connected to the C_{SUB} pin is not grounded.
3. The blooming signal generated during exposure in mechanical shutter mode is swept by providing two fields or more of idle transfer through vertical register high-speed sweep transfer from the time the mechanical shutter closes until sensor readout is performed. However, note that the V_L potential and the φSUB pin DC voltage sag at this time.

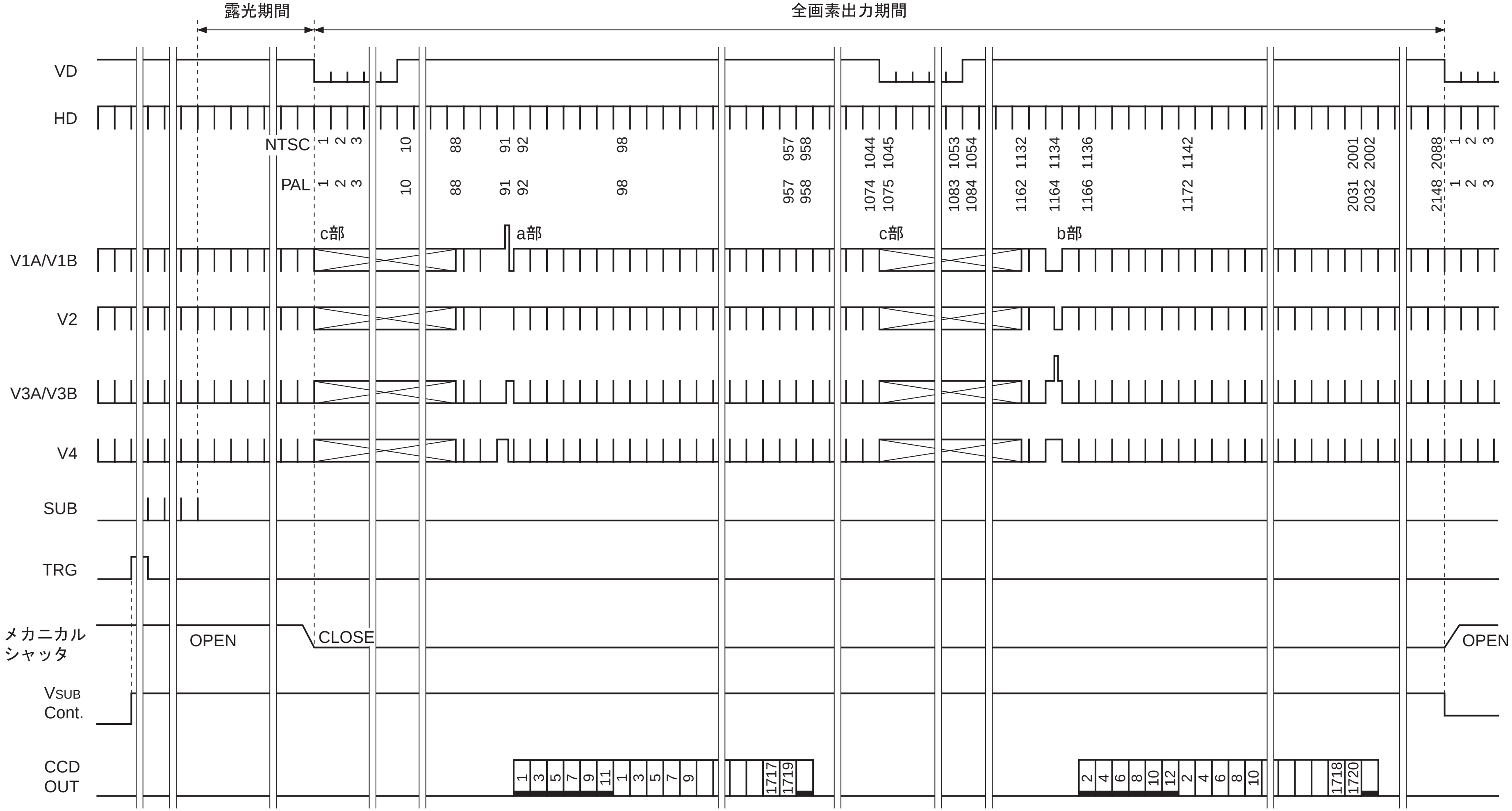
Drive Timing Chart (Vertical Sequence) High Frame Rate Readout Mode → Frame Readout Mode/Electronic Shutter Normal Operation


Act.
高速ドラフトモード
露光動作
フレーム読み出しモード
高速ドラフトモード
VD
V1A
V1B
V2
V3A
V3B
V4
SUB
A
B
B
C
D
E
TRG
メカニカル
シャッタ
OPEN
CLOSE
OPEN
VSUB
Cont.
CCD
OUT
A信号出力
A信号出力
B信号出力
B信号出力
C信号出力 (ODD)
C信号出力 (EVEN)
フレーム読み出し
後の出力
D信号出力
E信号出力

Note) The B output signals contain a blooming component and should therefore not be used.
Apply 20 or more electronic shutter pulses at the start of exposure for the recording image.
If less than 20 pulses are applied, the electronic shutter may occur a discharge error.

Drive Timing Chart (Vertical Sync) NTSC/PAL Frame Readout Mode

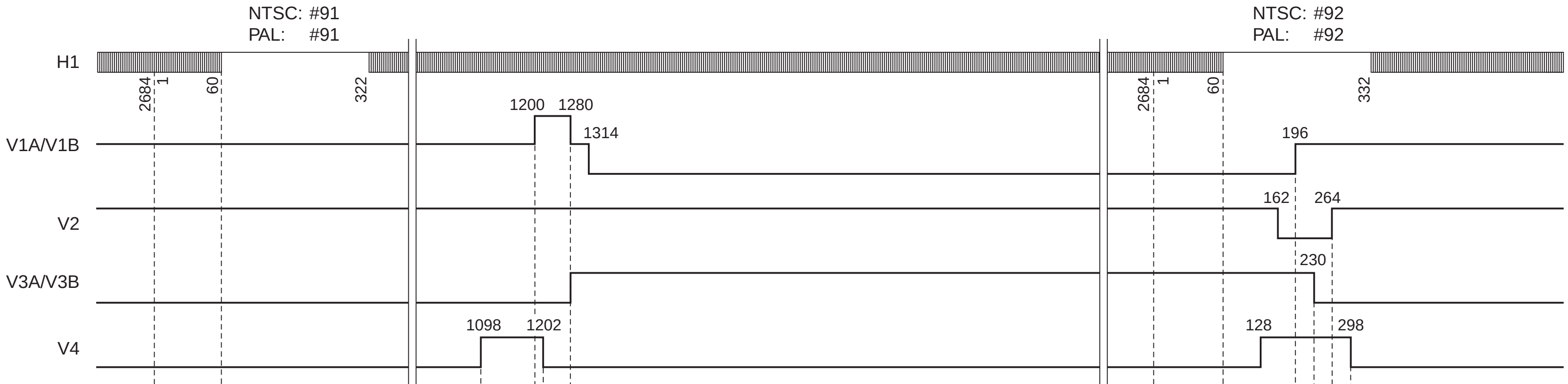
NTSC: 4.28 frame/s, PAL: 4.17 frame/s


露光期間
全画素出力期間
VD
HD
NTSC 1 2 3 10 88 91 92 98 957 958 1044 1045 1053 1054 1132 1134 1136 1142 2001 2002 2088 1 2 3
PAL 1 2 3 10 88 91 92 98 957 958 1074 1075 1083 1084 1162 1164 1166 1172 2031 2032 2148 1 2 3
c部
a部
c部
b部
V1A/V1B
V2
V3A/V3B
V4
SUB
TRG
メカニカル
シャッタ
OPEN
CLOSE
OPEN
VSUB
Cont.
CCD
OUT
1 3 5 7 9 11 1 3 5 7 9 1717 1719
2 4 6 8 10 12 2 4 6 8 10 1718 1720

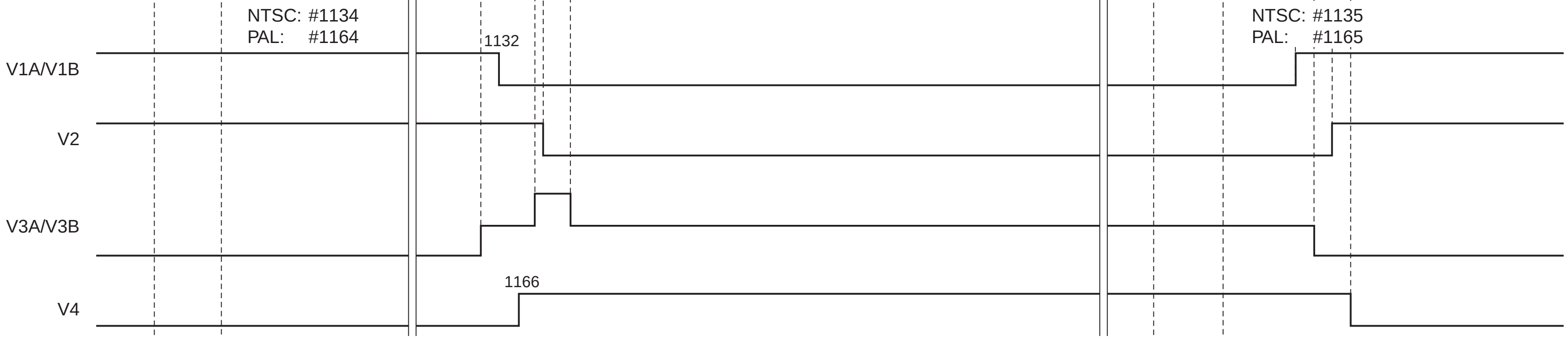
Note) The 1044 and 2088H horizontal period in NTSC mode are 938clk, the 1073H, 1074H, 2147H and 2148H horizontal period in PAL mode are 1376clk.

Drive Timing Chart (Readout) NTSC/PAL Frame Readout Mode

"a" Enlarged

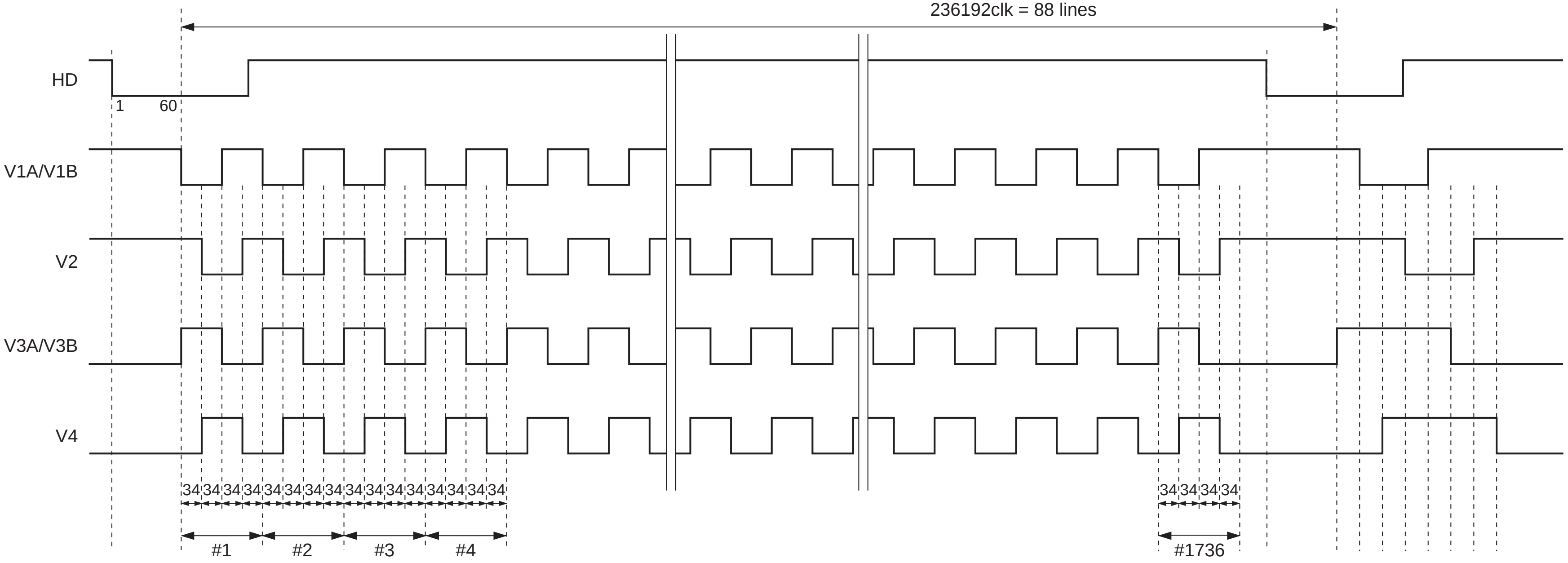

NTSC: #91
PAL: #91
NTSC: #92
PAL: #92
H1
2684
1
60
322
2684
1
60
332
V1A/V1B
1200
1280
1314
196
V2
162
264
V3A/V3B
230
V4
1098
1202
128
298

"b" Enlarged

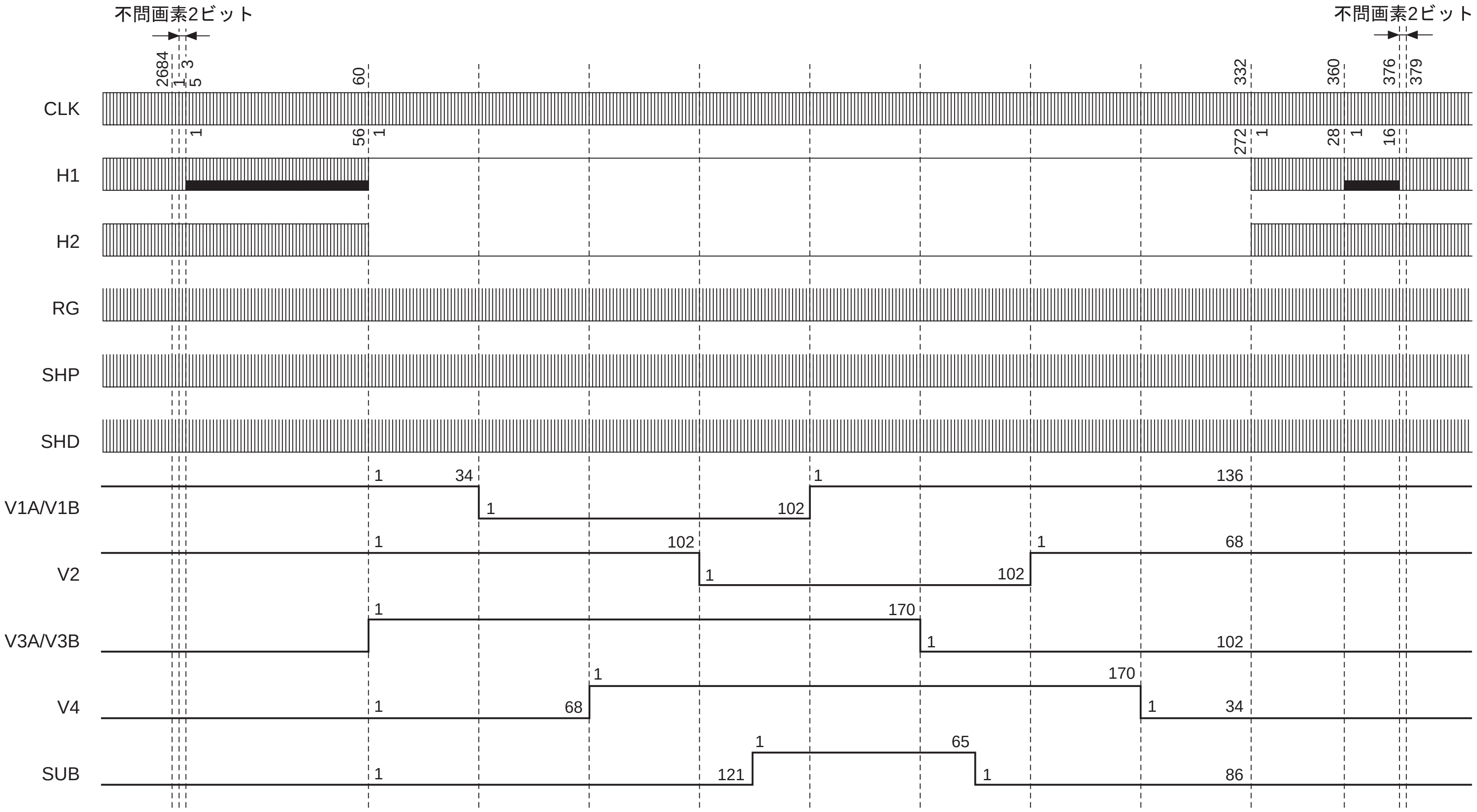

NTSC: #1134
PAL: #1164
NTSC: #1135
PAL: #1165
V1A/V1B
1132
V2
V3A/V3B
V4
1166

Drive Timing Chart (High-speed Sweep Operation) NTSC/PAL Frame Readout Mode

"c" Enlarged

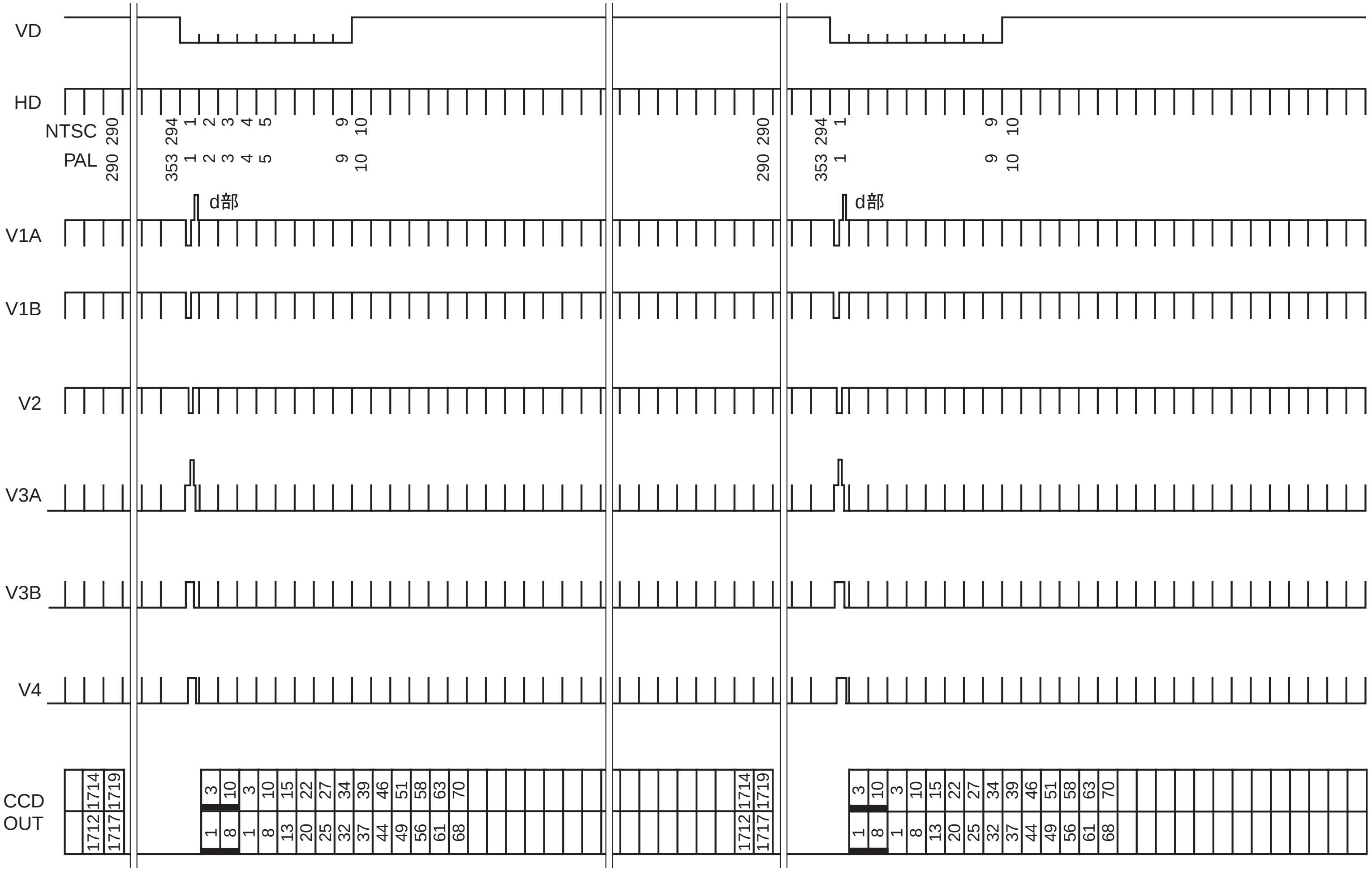

236192clk = 88 lines
HD
1
60
V1A/V1B
V2
V3A/V3B
V4
34 34 34 34 34 34 34 34 34 34 34 34 34 34 34 34
34 34 34 34
#1
#2
#3
#4
#1736

Drive Timing Chart (Horizontal Sync) NTSC/PAL Frame Readout Mode


不問画素2ビット
不問画素2ビット
2684
1
3
5
60
332
360
376
379
1
56
1
272
1
28
1
16
CLK
H1
H2
RG
SHP
SHD
V1A/V1B
1
34
1
102
1
136
V2
1
102
1
102
1
68
V3A/V3B
1
170
1
102
V4
1
68
1
170
1
34
SUB
1
121
1
65
1
86

Drive Timing Chart (Vertical Sync)   NTSC/PAL High Frame Rate Readout Mode

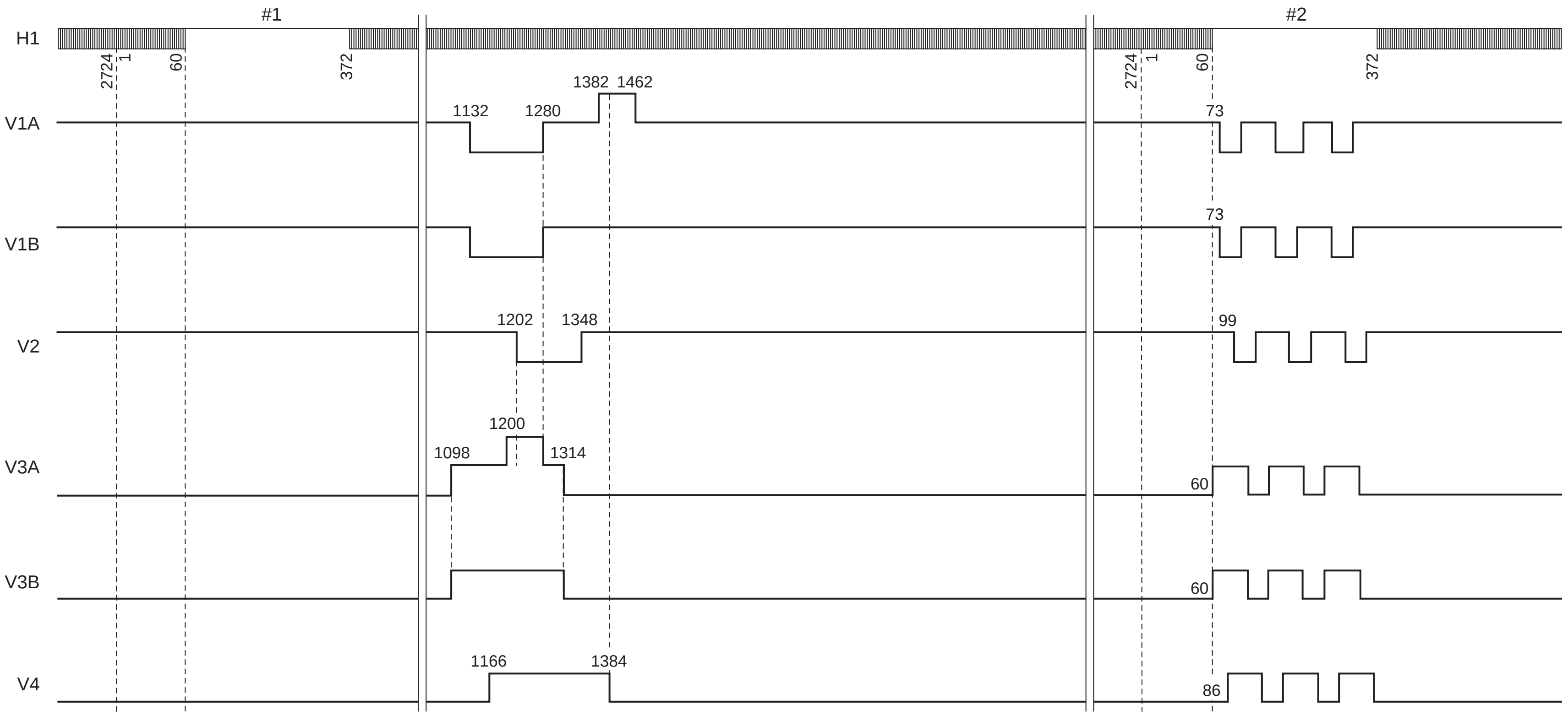
NTSC: 30 frame/s, PAL: 25 frame/s


VD
HD
NTSC 290 294 1 2 3 4 5 9 10 290 294 1 9 10
PAL 290 353 1 2 3 4 5 9 10 290 353 1 9 10
d部
V1A
V1B
V2
V3A
V3B
V4
CCD OUT
1714 1719 3 10 3 10 15 22 27 34 39 46 51 58 63 70
1712 1717 1 8 1 8 13 20 25 32 37 44 49 56 61 68
1714 1719 3 10 3 10 15 22 27 34 39 46 51 58 63 70
1712 1717 1 8 1 8 13 20 25 32 37 44 49 56 61 68

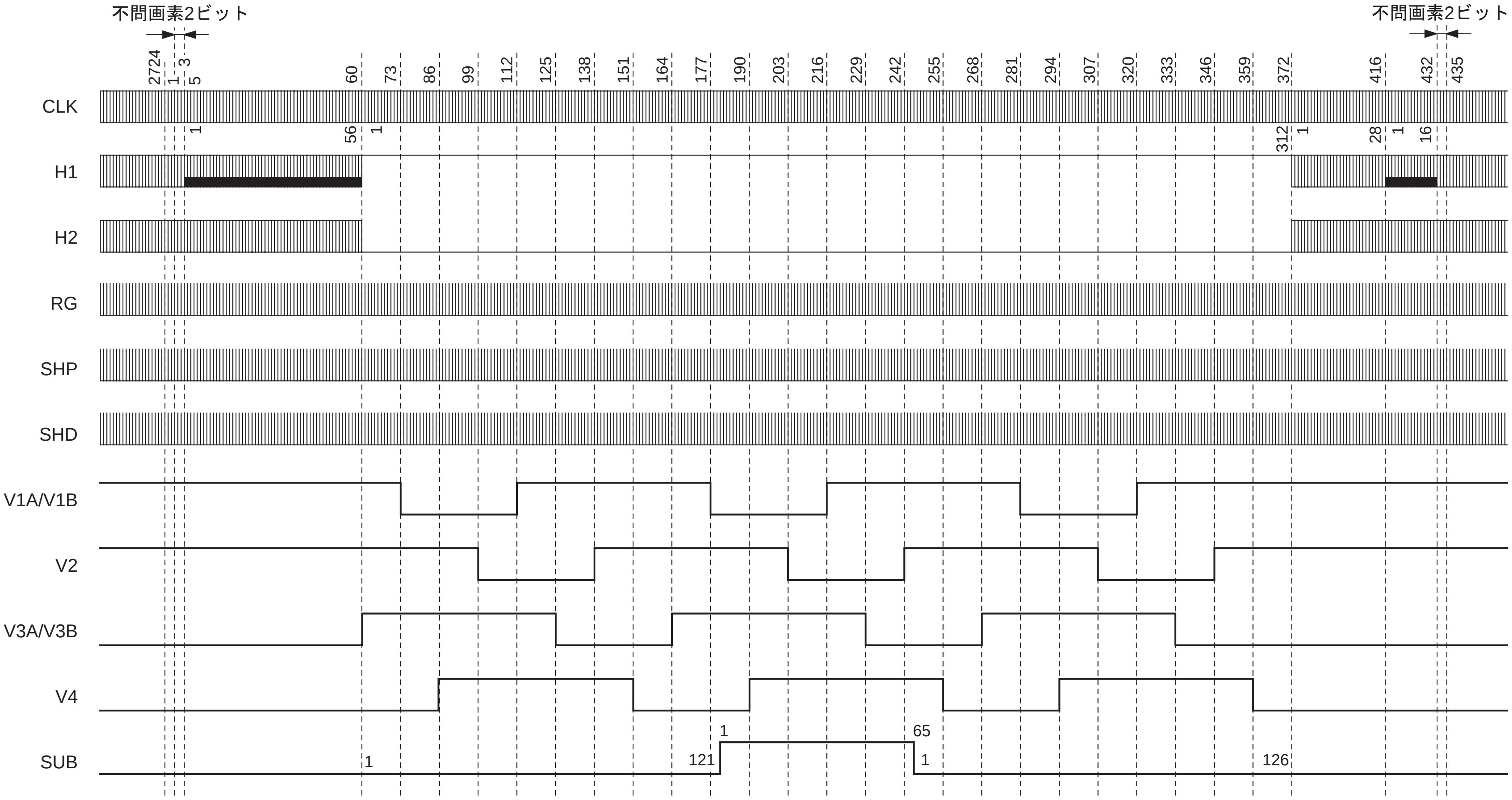
Note) The 294H horizontal period in NTSC mode are 1968clk, the 353H in PAL mode is 1152clk.

Drive Timing Chart (Readout) NTSC/PAL High Frame Rate Readout Mode, AF1 Mode, AF2 Mode

"d" Enlarged

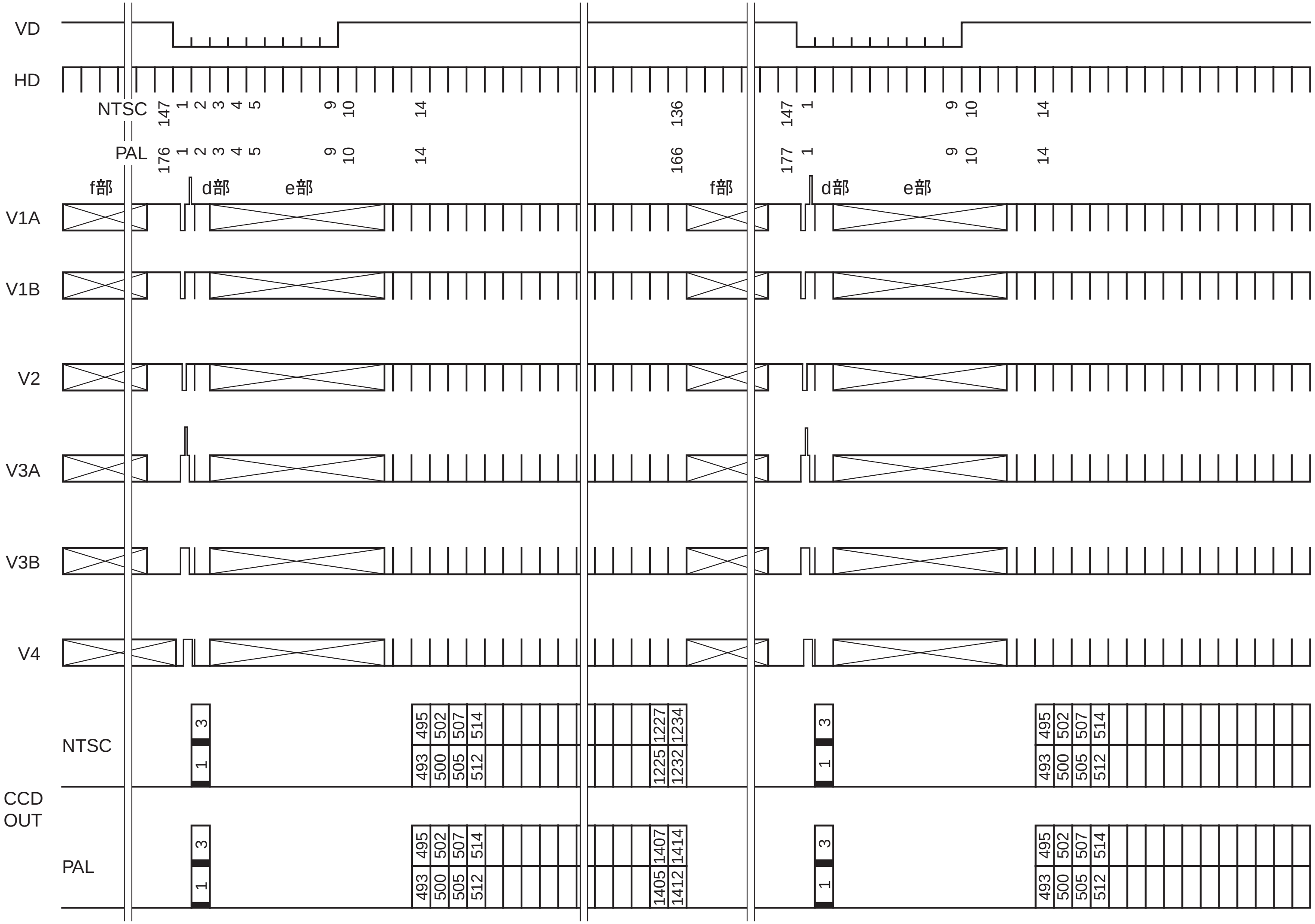

#1
#2
H1
2724
1
60
372
V1A
1132
1280
1382
1462
73
V1B
73
V2
1202
1348
99
V3A
1098
1200
1314
60
V3B
60
V4
1166
1384
86

Drive Timing Chart (Horizontal Sync) NTSC/PAL High Frame Rate Readout Mode, AF1 Mode, AF2 Mode


不問画素2ビット
不問画素2ビット
2724
1
3
5
60
73
86
99
112
125
138
151
164
177
190
203
216
229
242
255
268
281
294
307
320
333
346
359
372
416
432
435
CLK
1
56
1
312
1
28
1
16
H1
H2
RG
SHP
SHD
V1A/V1B
V2
V3A/V3B
V4
SUB
1
121
1
65
1
126

Drive Timing Chart (Vertical Sync) NTSC/PAL AF1 Mode

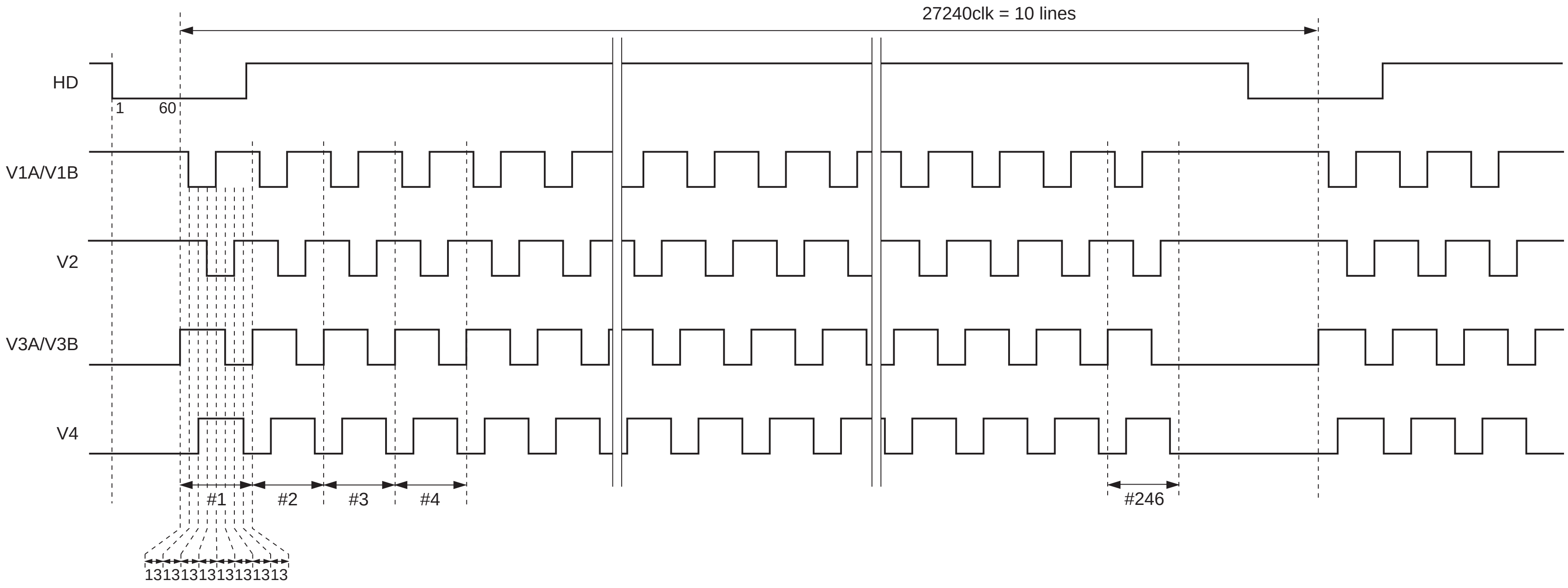
NTSC: 60 frame/s, PAL: 50 frame/s


VD
HD
NTSC
147 1 2 3 4 5 9 10 14 136 147 1 9 10 14
PAL
176 1 2 3 4 5 9 10 14 166 177 1 9 10 14
f部
d部
e部
V1A
V1B
V2
V3A
V3B
V4
CCD OUT
NTSC
3
1
495 502 507 514 1227 1234
493 500 505 512 1225 1232
PAL
495 502 507 514 1407 1414
493 500 505 512 1405 1412

Note) The 147H horizontal period in NTSC mode are 2346clk, the 177H in PAL mode is 576clk.

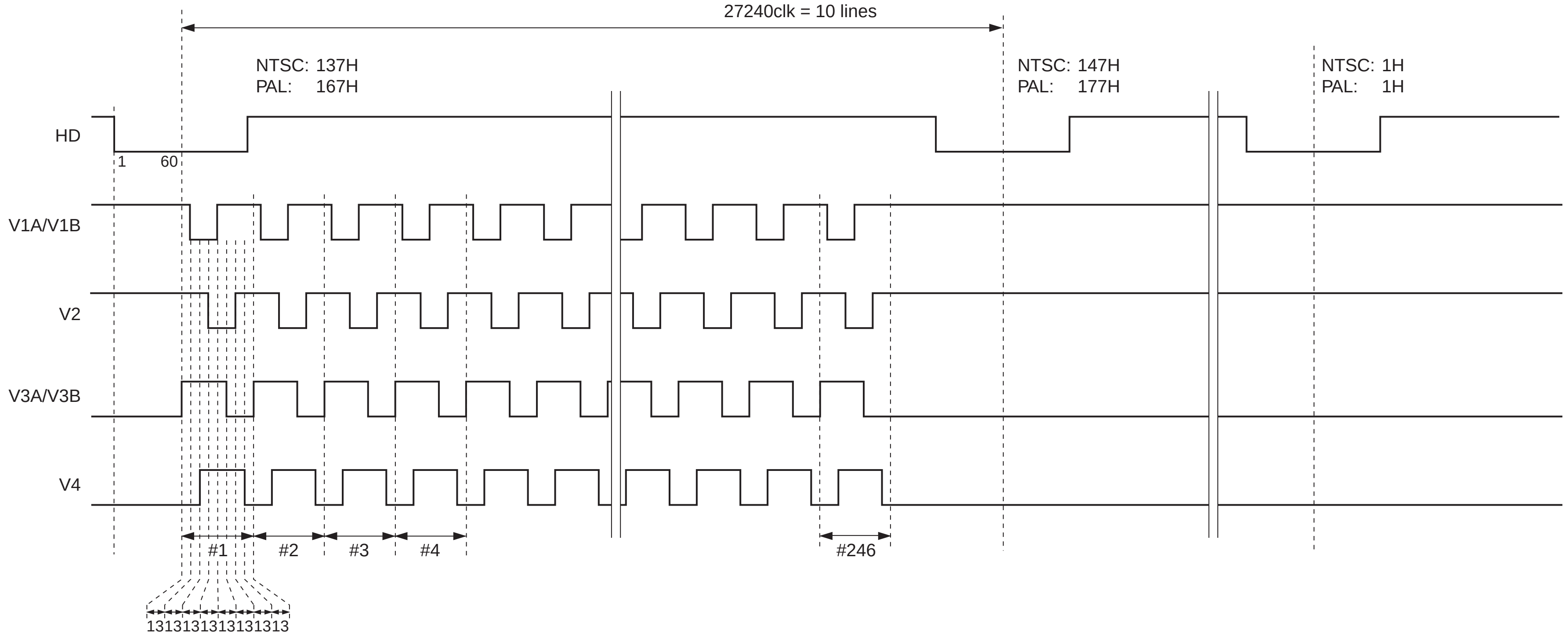
Drive Timing Chart NTSC/PAL AF1 Mode

"e" Enlarged


27240clk = 10 lines
HD
1
60
V1A/V1B
V2
V3A/V3B
V4
#1
#2
#3
#4
#246
13
13
13
13
13
13
13
13

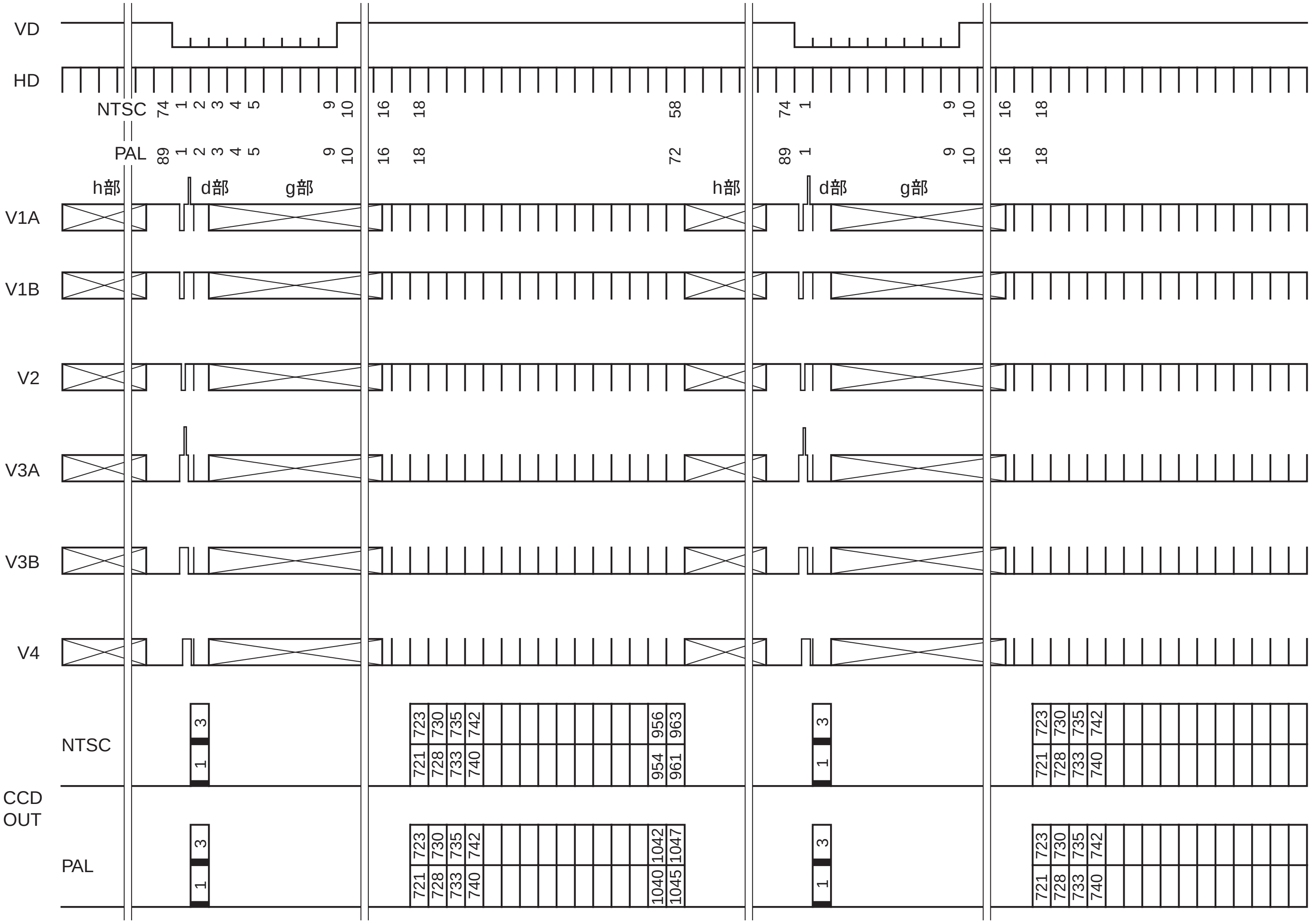
Drive Timing Chart NTSC/PAL AF1 Mode, AF2 Mode

"f" Enlarged


27240clk = 10 lines
NTSC: 137H
PAL: 167H
NTSC: 147H
PAL: 177H
NTSC: 1H
PAL: 1H
HD
1
60
V1A/V1B
V2
V3A/V3B
V4
#1
#2
#3
#4
#246
13
13
13
13
13
13
13
13

Drive Timing Chart (Vertical Sync) NTSC/PAL AF2 Mode

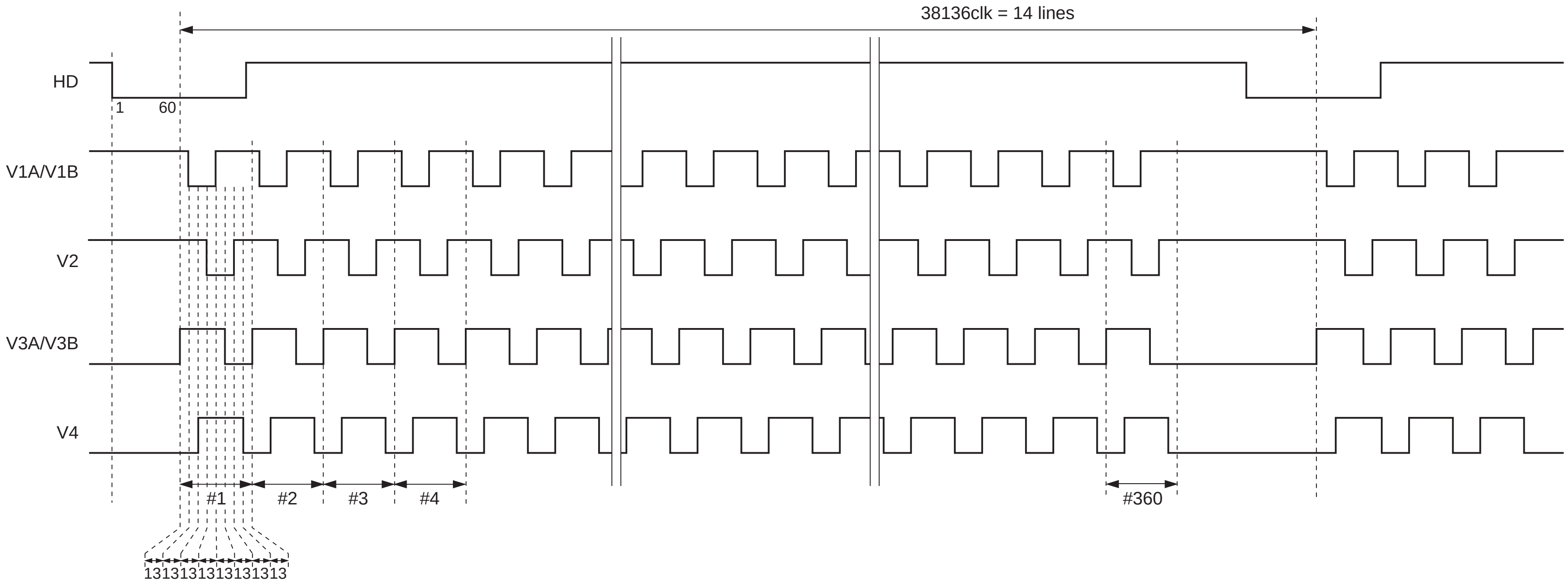
NTSC: 120 frame/s, PAL: 100 frame/s


VD
HD
NTSC 74 1 2 3 4 5 9 10 16 18 58 74 1 9 10 16 18
PAL 89 1 2 3 4 5 9 10 16 18 72 89 1 9 10 16 18
h部 d部 g部 h部 d部 g部
V1A
V1B
V2
V3A
V3B
V4
CCD OUT
NTSC
3 1
723 730 735 742 956 963
721 728 733 740 954 961
PAL
3 1
723 730 735 742 1042 1047
721 728 733 740 1040 1045

Note) The 74H horizontal period in NTSC mode are 1173clk, the 88H and 89H in PAL mode is 1506clk.

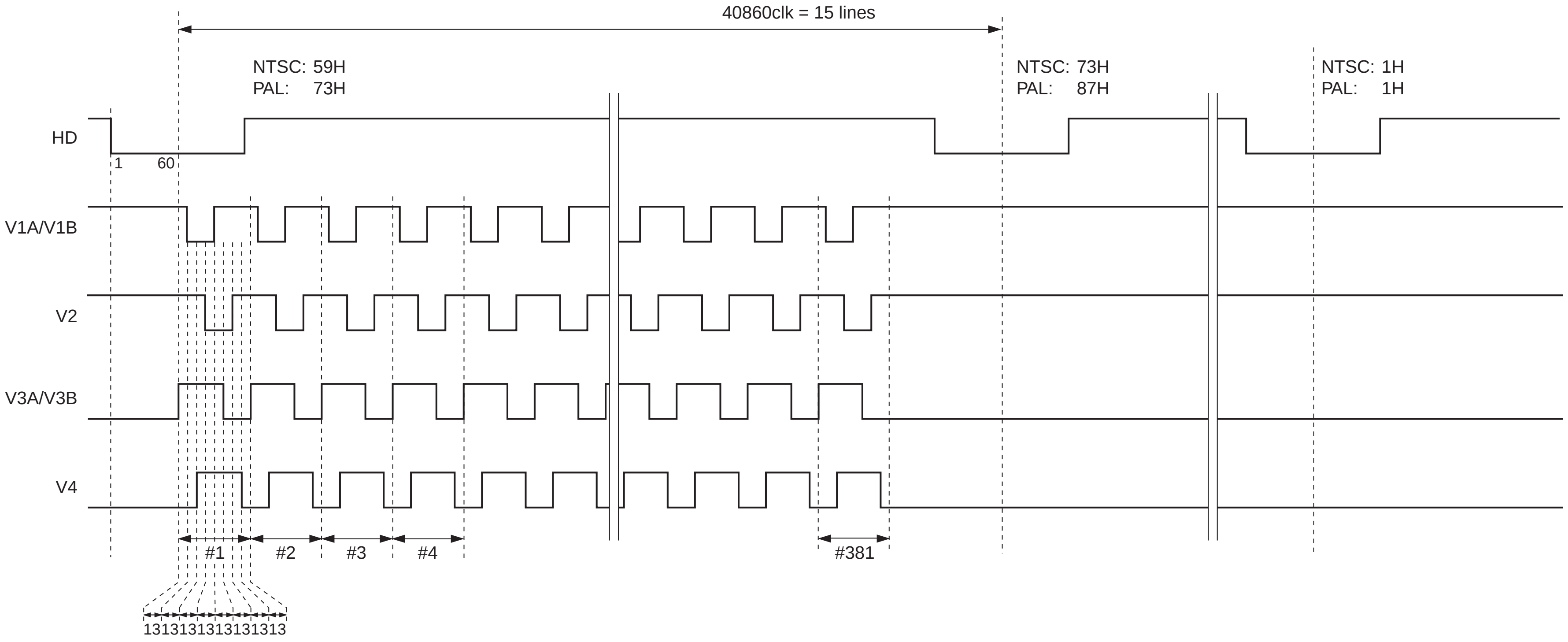
Drive Timing Chart NTSC/PAL AF2 Mode

"g" Enlarged


38136clk = 14 lines
HD
1
60
V1A/V1B
V2
V3A/V3B
V4
#1
#2
#3
#4
#360
1313131313131313

Drive Timing Chart NTSC/PAL AF2 Mode

"h" Enlarged


40860clk = 15 lines
NTSC: 59H
PAL: 73H
NTSC: 73H
PAL: 87H
NTSC: 1H
PAL: 1H
HD
1
60
V1A/V1B
V2
V3A/V3B
V4
#1
#2
#3
#4
#381
1313131313131313

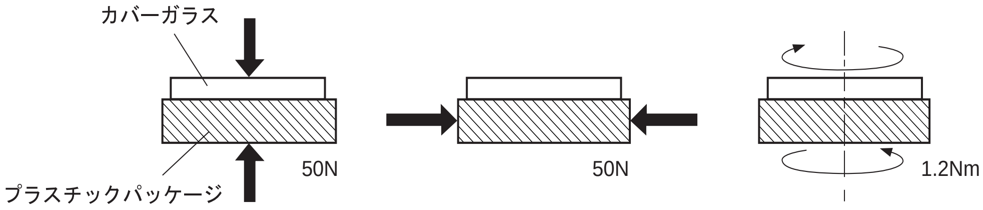
Notes on Handling

1) Static charge prevention
   CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.
   a) Either handle bare handed or use non-chargeable gloves, clothes or material.
      Also use conductive shoes.
   b) When handling directly use an earth band.
   c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
   d) Ionized air is recommended for discharge when handling CCD image sensors.
   e) For the shipment of mounted substrates, use boxes treated for the prevention of static charges.

2) Soldering
   a) Make sure the package temperature does not exceed 80°C.
   b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a 30W soldering iron with a ground wire and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
   c) To dismount an image sensor, do not use a solder suction equipment. When using an electric desoldering tool, use a thermal controller of the zero-cross On/Off type and connect it to ground.

3) Dust and dirt protection
   Image sensors are packed and delivered by taking care of protecting its glass plates from harmful dust and dirt. Clean glass plates with the following operations as required, and use them.
   a) Perform all assembly operations in a clean room (class 1000 or less).
   b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)
   c) Clean with a cotton bud and ethyl alcohol if grease stained. Be careful not to scratch the glass.
   d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
   e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

4) Installing (attaching)
   a) Remain within the following limits when applying a static load to the package. Do not apply any load more than 0.7mm inside the outer perimeter of the glass portion, and do not apply any load or impact to limited portions. (This may cause cracks in the package.)



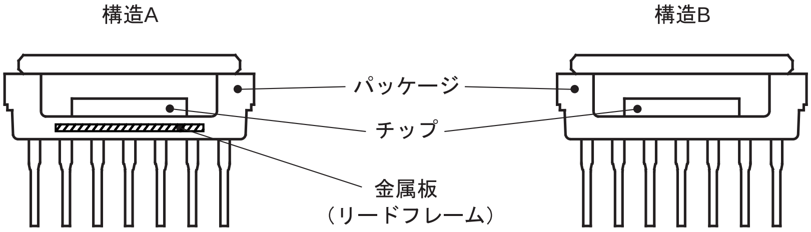
圧縮力　　ひねりトルク

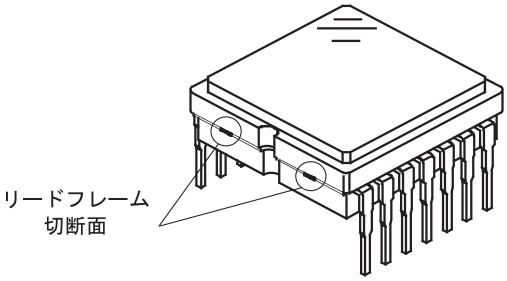
   b) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package. Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.

- c) The adhesive may cause the marking on the rear surface to disappear, especially in case the regulated voltage value is indicated on the rear surface. Therefore, the adhesive should not be applied to this area, and indicated values should be transferred to other locations as a precaution.
- d) The notch of the package is used for directional index, and that can not be used for reference of fixing. In addition, the cover glass and seal resin may overlap with the notch of the package.
- e) If the leads are bent repeatedly and metal, etc., clash or rub against the package, the dust may be generated by the fragments of resin.
- f) Acrylate anaerobic adhesives are generally used to attach CCD image sensors. In addition, cyano-acrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives. (reference)

5) Others

- a) Do not expose to strong light (sun rays) for long periods, as color filters will be discolored. When high luminous objects are imaged with the exposure level controlled by the electronic iris, the luminance of the image-plane may become excessive and discoloring of the color filter will possibly be accelerated. In such a case, it is advisable that taking-lens with the automatic-iris and closing of the shutter during the power-off mode should be properly arranged. For continuous using under cruel condition exceeding the normal using condition, consult our company.
- b) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.
- c) Brown stains may be seen on the bottom or side of the package. But this does not affect the CCD characteristics.
- d) This package has 2 kinds of internal structure. However, their package outline, optical size, and strength are the same.

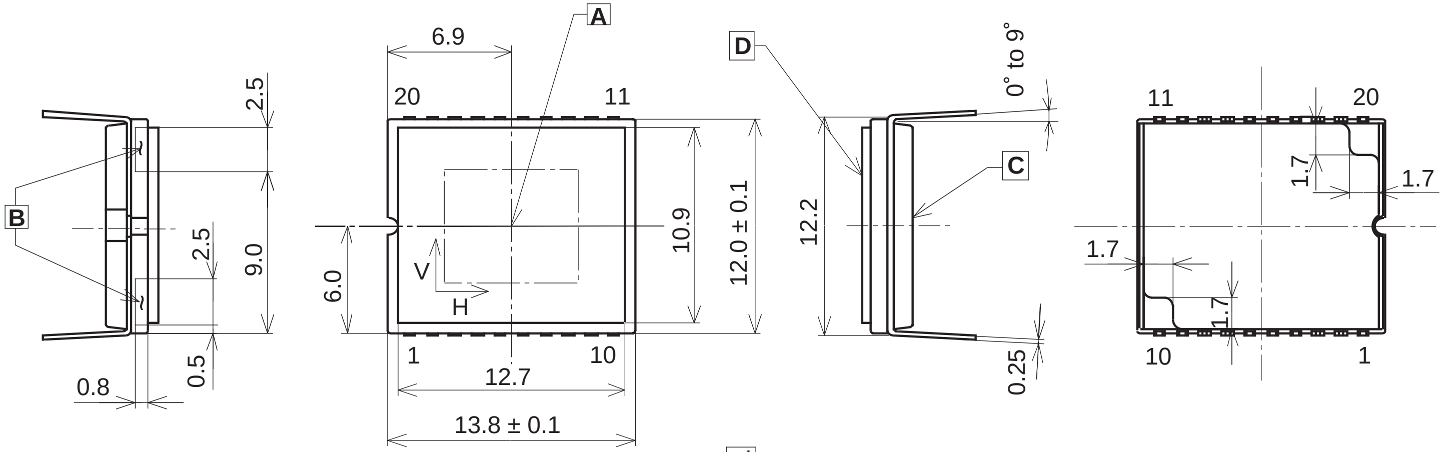


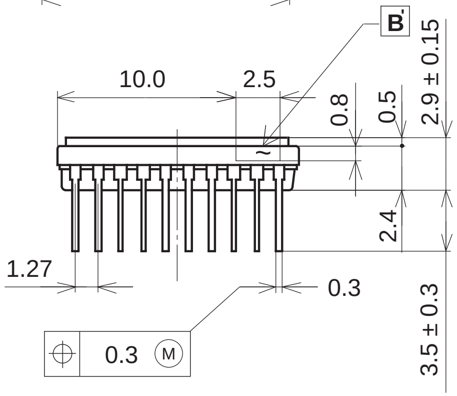


The cross section of lead frame can be seen on the side of the package for structure A.

Package Outline Unit: mm

20 pin DIP





1. **“A”** is the center of the effective image area.
2. The two points **“B”** of the package are the horizontal reference.
   The point **“B'”** of the package is the vertical reference.
3. The bottom **“C”** of the package, and the top of the cover glass **“D”** are the height reference.
4. The center of the effective image area relative to **“B”** and **“B'”** is (H, V) = (6.9, 6.0) ± 0.075mm.
5. The rotation angle of the effective image area relative to H and V is ± 1°.
6. The height from the bottom **“C”** to the effective image area is 1.41 ± 0.10mm.
   The height from the top of the cover glass **“D”** to the effective image area is 1.49 ± 0.15mm.
7. The tilt of the effective image area relative to the bottom **“C”** is less than 50µm.
   The tilt of the effective image area relative to the top **“D”** of the cover glass is less than 50µm.
8. The thickness of the cover glass is 0.5mm, and the refractive index is 1.5.
9. The notches on the bottom of the package are used only for directional index, they must not be used for reference of fixing.

PACKAGE STRUCTURE

PACKAGE MATERIAL	Plastic
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	0.95g
DRAWING NUMBER	AS-B6-04(E)