S5K2E1FX03_EVT2

(1/2.5” QSXGA CMOS Image Sensor)

Preliminary Data Sheet

(Rev 0.00)

DOCUMENT REVISION HISTORY

Versoin	Date	Amendment
0.00	06-06-01	EVT2 Initial draft.

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FEATURES

Optical size: 1/2.5 inch
Pixel size: 2.20 um
Effective resolution: 2608 (H) x 1952 (V), QSXGA
Line progressive read out
Vertical and horizontal flip mode
Continuous frame capture mode
Sub-sampled readout (x2, x4, x8)
Average Sub-sampled readout (x2)
Output format: RAW 8/10/12/13-bit (10-bit is default, 13-bit mode is only for test)
Max. frame rate: 10fps @ QSXGA
Operating temperature: -30°C to +70°C
Supply voltage: 2.8V for analog 1.8V for digital
Internal voltage regulator for 1.5V generation
Internal PLL for high speed clock generation
Internal Scaler for generating lower resolution full field of view image without loss of image quality

GENERAL DESCRIPTION

The S5K2E1FX03 is a highly integrated CMOS image sensor fabricated by SAMSUNG 0.13μm CMOS image sensor process. It is developed for imaging application to realize high-efficiency and low-power photo sensor. The sensor consists of 2608 x 1952 effective pixels which meet with 1/2.5 inch optical format. The sensor has on-chip 12-bit ADC blocks to digitize the pixel output and also on-chip Correlated Double Sampling (CDS) to reduce Fixed Pattern Noise (FPN) drastically. With its few interface signals and 12-bit raw data directly connected to the external devices, a camera system can be configured easily.

PIN DESCRIPTION

Table 1: Chip PAD Description

Pin No	Pin Name	I/O	Description
1	**STBYN**	I	Stand-by control signal (active low)
2	**STRB**	I	Control signal for strobe (active high)
3	**REG_CAP**	O	External cap (1uF) connected to DGND
8~18	**D0~D10**	O	Parallel pixel data output. D0 : LSB, D12 : MSB
21,22	**D11,D12**	O	
23	**PCLK**	O	Pixel clock output
24	**VSYNC**	O	Vertical sync output
25	**HSYNC**	O	Horizontal sync output
26	**SCE**	I	Control signal for test mode. internal pull-down
33	**REF_R**	O	External reference resistor(12kΩ) connected to analog ground
34	**MCLK**	I	External input clock
43	**NC (TCLK2)**	I	No Connection (Control signal for test mode. internal pull-down)
44	**NC (TCLK1)**	I	No Connection (Control signal for test mode. internal pull-down)
47	**NC (PLL_FLT)**	O	No Connection (PLL loop filter voltage monitoring)
49	**TST_DBLR**	O	Analog voltage PAD. External cap(0.1uF) connected to VSSA
50	**TST_PIXEL**	O	Analog voltage PAD. External cap(0.1uF) connected to VSSA
51	**NC (REF_IN)**	I	No Connection (input for ADC test)
52	**NC (SIG_IN)**	I	No Connection (input for ADC test)
76	**VPAD2**	I	Analog voltage PAD. External cap(1uF) connected to VSSA
78	**TST2**	I	Control signal for test mode. must connect to VDDA.
79	**TST1**	I	Control signal for test mode. must connect to VSSA.
80	**TST0**	I	Control signal for test mode. must connect to VSSA.
83	**SCL**	B	IIC clock signal
84	**SDA**	B	IIC data signal
31,45, 54,74, 82	**VDDA**	P	Analog Power (2.8V)
32,46, 53,75, 81	**VSSA**	P	Analog Ground
4,6,19 ,36,42	**VDDD**	P	Digital Power (1.8V)
5,7,20 ,35,41 ,48,77	**VSSD**	P	Digital Ground

PIN CONFIGURATION

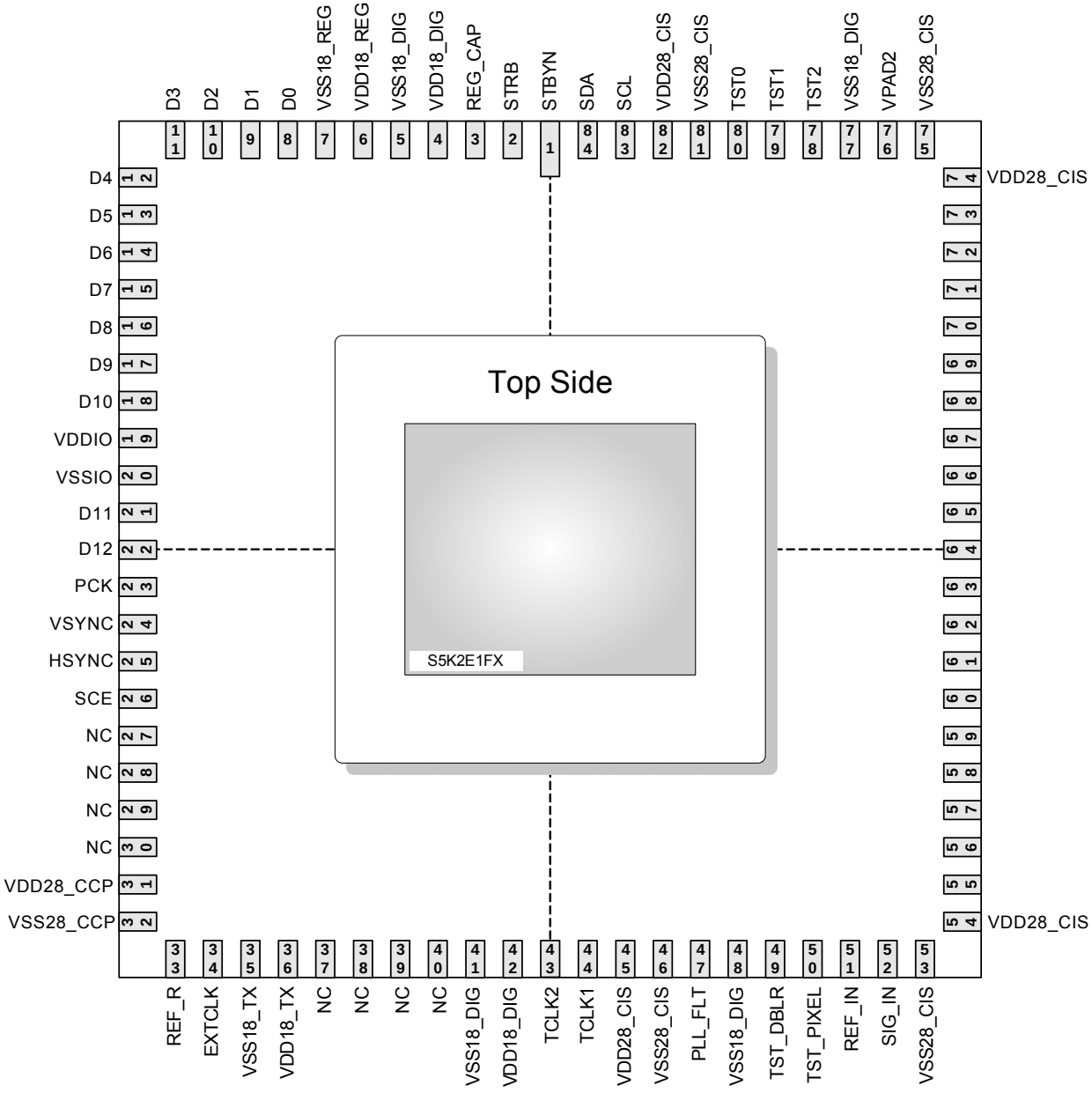


Figure 1: Pin Configuration

PIXEL ARRAY INFORMATION

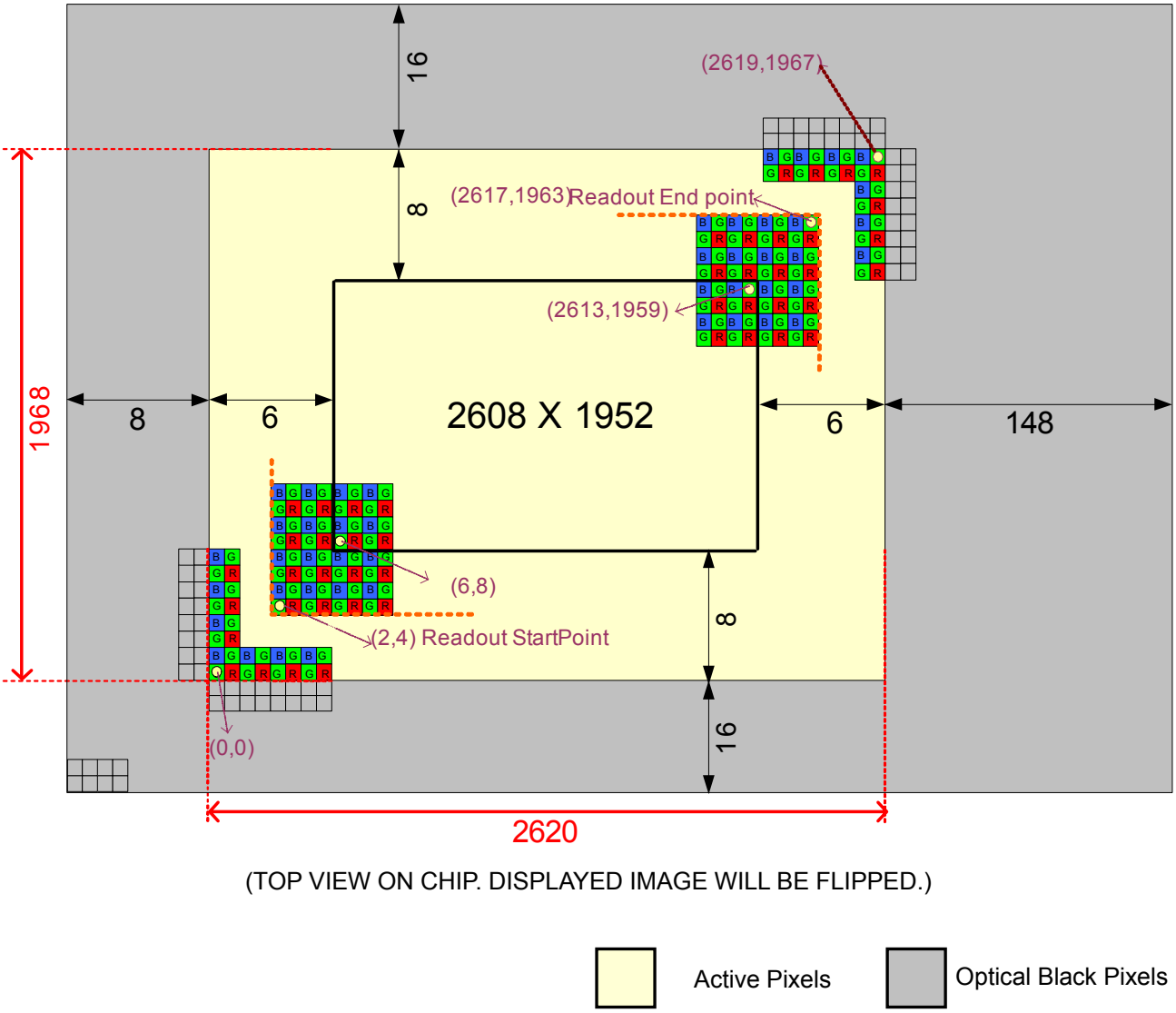


Figure 2: Pixel Array Information

FUNCTIONAL DESCRIPTION

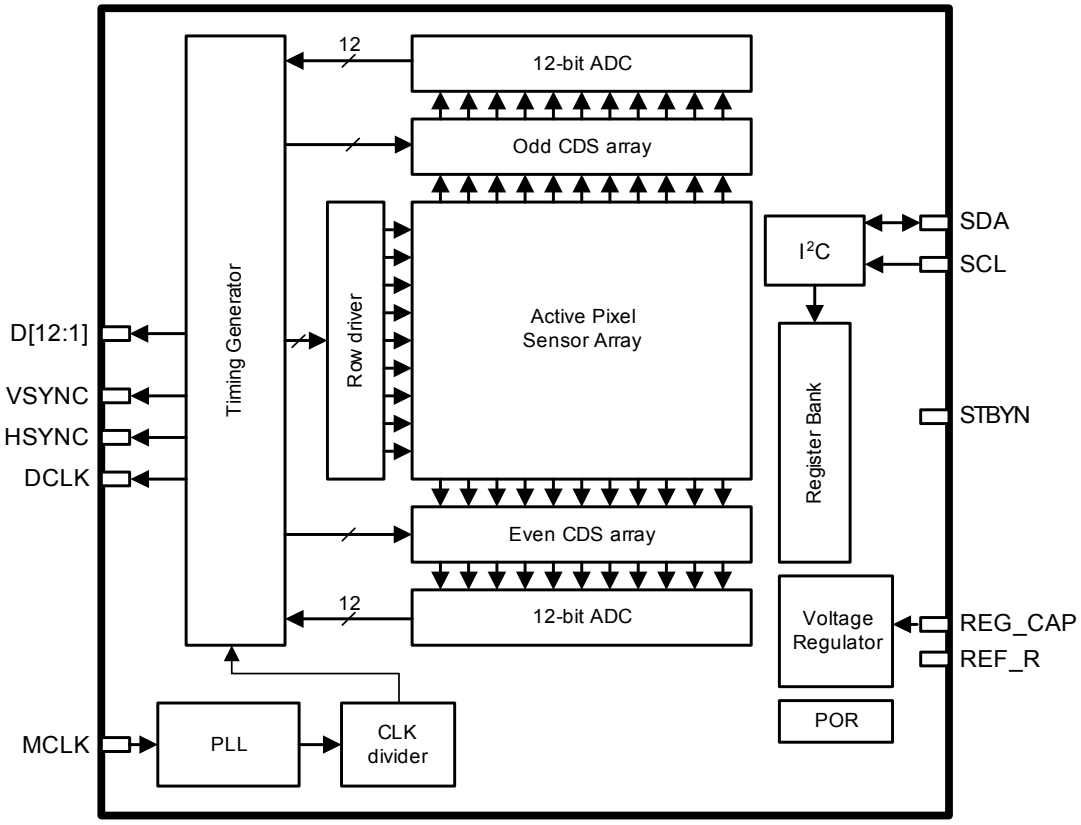


Figure 3: Function Block Diagram

1. Output Data Format

1-1. Synchronous Signal Output

The horizontal sync(HSYNC) and vertical sync(VSYNC) signals are also available. The sync pulse width, polarity and position are programmable by control registers (ref. timing chart). When display mode is enabled, the sync signal outputs indicate that the output data is valid (**hsdisp**=1) or the output rows are valid (**vsdisp**=1).
In default register setting, the output format is RAW 10-bit. the output formats can be selected among RAW 8/10/12-bit by setting **adc_res** register(Bit[3:2] of Reg0x02).

In each output format, the output pin mapping is as follows.

Output format	Output pin	adc_res [3:2]	Description
RAW 8-bit	D12 (MSB) ~ D5 (LSB)	00b	The unused output pins are in low state.
RAW 10-bit	D12(MSB) ~ D3 (LSB)	01b	
Raw 12-bit	D12 (MSB) ~ D1 (LSB)	10b	

1-2. Pixel array addresses

Addressable pixel array is defined as the pixel address range to be read. The Addressable pixel array can be assigned anywhere on the pixel array. The addressed region of the pixel array is controlled by **x_addr_start**, **y_addr_start**, **x_addr_end** and **y_addr_end** register. Figure 4 refers to a pictorial representation of the Addressable pixel array on the Physical pixel array

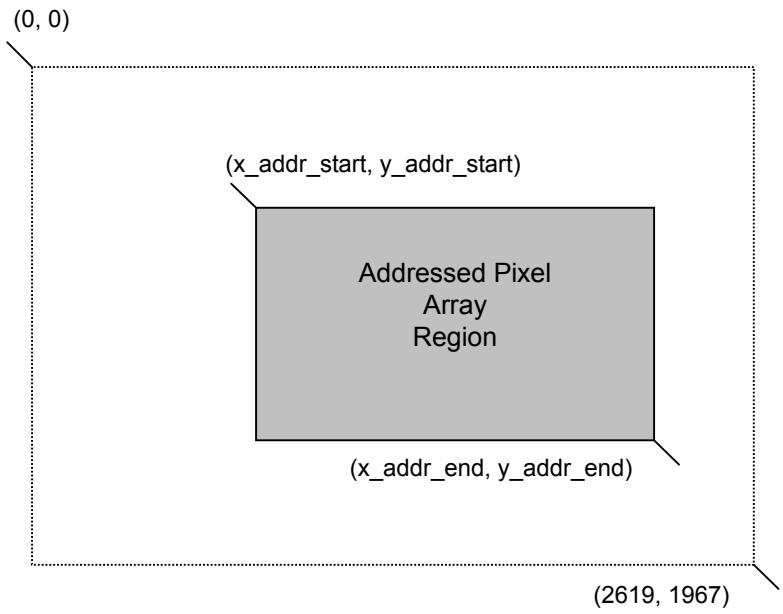


Figure 4: Physical Pixel Array

Figure 5 refers to a Window of interest setting guide on the Physical pixel array

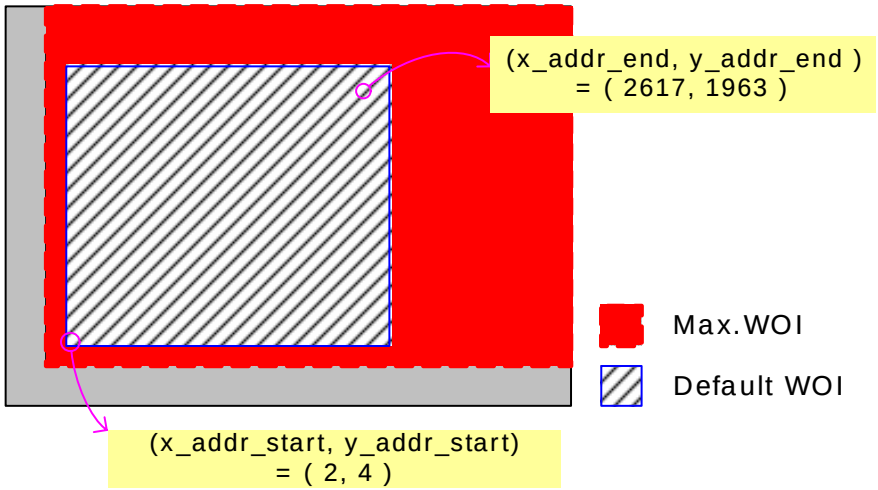


Figure 5: WOI(Window of interest) setup

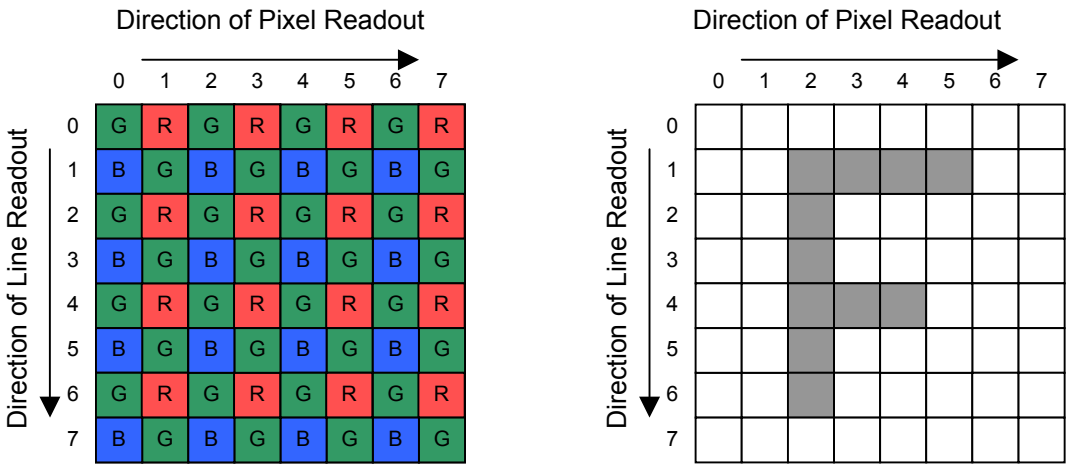
[NOTE]
(1) (x_addr_start, y_addr_start) : readout start pixel
(2) (x_addr_start, y_addr_end) : readout end pixel

1-3. Mirror/Flip

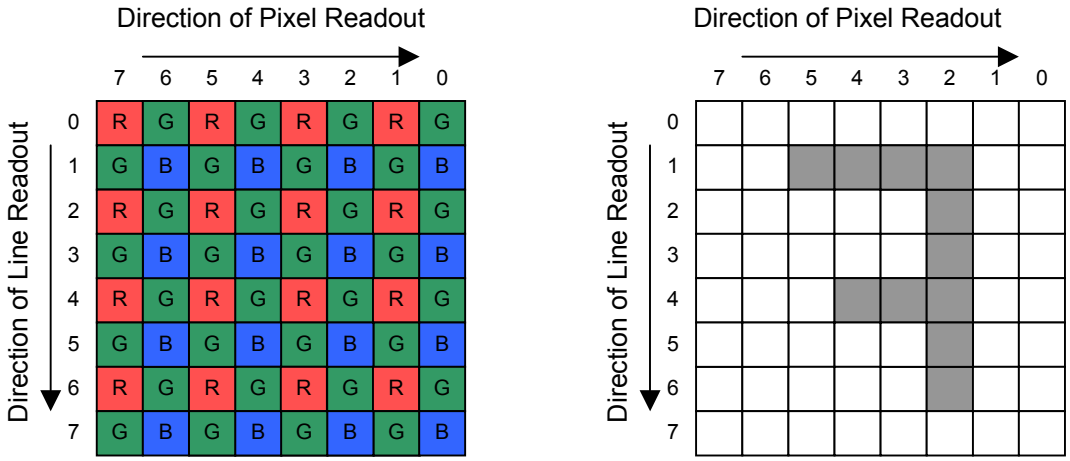
The pixel data are read out from left to right in horizontal direction and from top to bottom in vertical direction normally. By changing the mirror/flip mode, the read-out sequence can be reversed and the resulting image can be flipped like a mirror image. Pixel data are read out from right to left in horizontal mirror mode and from bottom to top in vertical flip mode. The horizontal mirror and the vertical flip mode can be programmed by image orientation register.

The sensor module support 4 possible pixel readout order

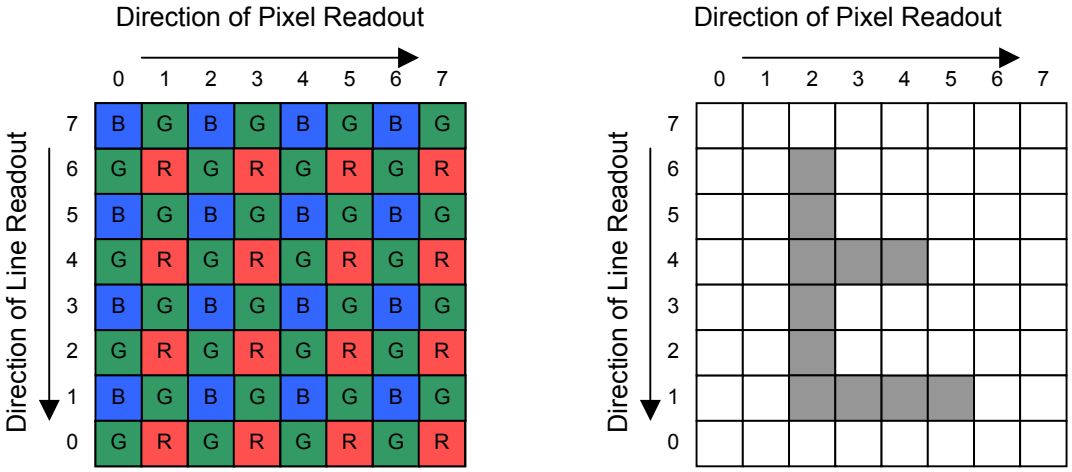
standard readout
Horizontally mirrored readout
Vertical Flipped readout
Horizontally Mirrored and Vertically Flipped readout



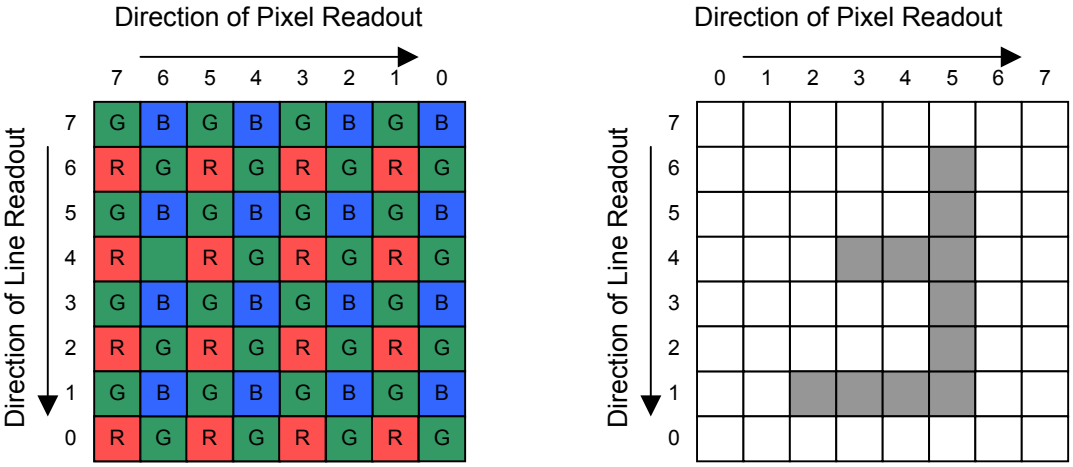
1) Standard Readout



2) Horizontally Mirrored Readout



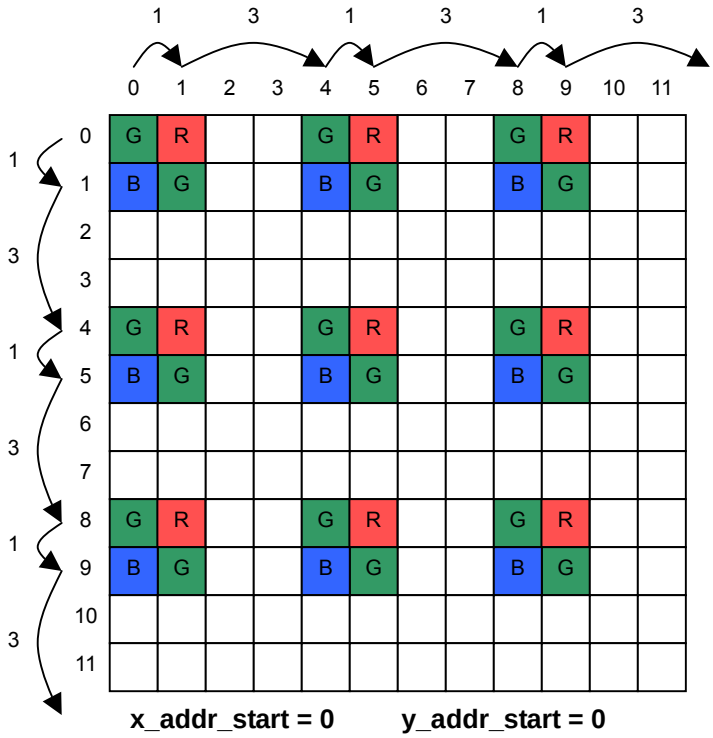
3) Vertically Flipped Readout



4) Horizontally Mirrored and Vertically Flipped Readout

1-4. Sub-Sampled readout

By programming the x and y odd and even increment register (**x_even_inc**, **x_odd_inc**, **y_even_inc**, **y_odd_inc**). the sensor can be configured to readout sub-sampled pixel data.



1-5. Frame Rate Control (Virtual Frame)

The line rate and the frame rate can be changed by varying the size of virtual frame. The virtual frame's width and depth are controlled by **line_length_pck** and **frame_length_lines** register. The frame rate can be calculated by the following equation:

Frame rate = 1 / (line_length_pck * frame_length_lines) * DCLK

For S5K2E1FX03, the minimum **line_length_pck** is 3176(decimal) and other parameters can be set appropriately according to the above equation.

Figure 6 refers to a Frame Format setting guide on the Physical pixel array

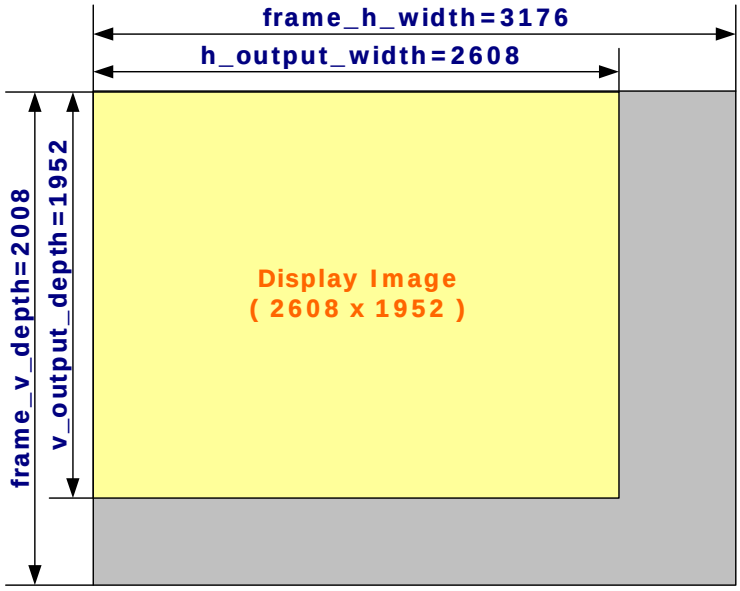


Figure 6: Frame Format setting guide

[NOTE]
(1) 1 Frame = frame_length_lines x line_length_pck
(2) line_length_pck = h_output_size + hblank
- hblank is decided by line_length_pck, h_output_size register
- line_length_pck > Min.line_length_pck
-

*Sub-sampling On/Off	adc_res[1:0]	Min. line_length_pck
Off	2'b00 (8bit)	3176
Off	2'b01 (10bit)	3176
Off	2'b10 (12bit)	3176
Off	2'b11 (13bit)	4912
On	2'b00 (8bit)	1868
On	2'b01 (10bit)	1968
On	2'b10 (12bit)	2864
On	2'b11 (13bit)	4912

* Sub-sampling Off : x_even_inc, x_odd_inc both are 1
* frame_length_lines = v_output_size + vblank
* vblank is decided by frame_length_lines, v_output_size register
* hblank and vblank have not specific register

Table 2: **Register setting guide for frame rate**

GROUP	Addr	Default	Register Name	Bits	Descriptions
ADC res	02h	04h	adc_res	[3:2]	Output data resolution control
Frame Timing	20h	07h	frame_length_line[15:0]	[7:0]	Frame length Units:Lines
	21h	D8h		[7:0]	
	22h	0Ch	line_length_pck[15:0]	[7:0]	Line length Units:Pixel clocks
	23h	68h		[7:0]	
Image Size	24h	00h	x_addr_start[11:0]	[7:0]	x_address of the top left corner of the visible pixel data Units:Pixels
	25h	02h		[7:0]	
	26h	00h	y_addr_start[11:0]	[7:0]	y_address of the top left corner of the visible pixel data Units:Lines
	27h	04h		[7:0]	
	28h	0Ah	x_addr_end[11:0]	[7:0]	x_address of the bottom right corner of the visible pixel data Units:Pixels
	29h	39h		[7:0]	
	2Ah	07h	y_addr_end[11:0]	[7:0]	y_address of the bottom right corner of the visible pixel data Units:Lines
	2Bh	ABh		[7:0]	
	2Ch	0Ah	x_output_size[11:0]	[7:0]	Width of image data output from the sensor module Units:Pixels
	2Dh	30h		[7:0]	
	2Eh	07h	y_output_size[11:0]	[7:0]	Height of image data output from the sensor module Units:Lines
	2Fh	A0h		[7:0]	

1-6. Integration Time Control (Electronic Shutter Control)

The pixel integration time is controlled by shutter operation. In shutter operation, the amount of time, integration time, is determined by the column Step Integration Time Control Register (**fine_integration_time**) and line Step Integration Time Control Register(**coarse_integration_time**). The total integration time of sensor module can be calculated using the following formula.

Total_integration_time =

{(coarse_integration_time*pixel_period_per_line)+fine_integration_time} * 1/DCLK

1-7. Continuous Frame Capture Mode(CFCM) Integration Time Control (Electronic Shutter Control)

In CFCM operation, the integration time is controlled by shutter operation. The shutter operation is done when shutter control register (**shut_ctrl**) is set to “1”. In shutter operation, the integration time is determined by the Row Step Integration Time Control Register(**coarse_integration_time**) and Column Step Integration Time Control Register(**fine_integration_time**).

2. Analog to Digital Converter (ADC)

The image sensor has an on-chip 12-bit ADC. Column parallel ADC scheme is used for low power analog processing. The default ADC resolution is 10-bit and D12 to D3 are used to output image data parallelly.

2-1. Correlated Double Sampling (CDS)

The analog output signal of each pixel includes some temporal random noise caused by the pixel reset action and some fixed pattern noise by the in-pixel amplifier offset deviation. To eliminate those noise components, a correlated double sampling(CDS) circuit is used before converting to digital. The output signal sampled twice, once for the reset level and once for the actual signal level sampling.

2-2. Analog Gain and Offset Control

The user can control the gain of pixel signal by analog gain control registers(**analogue_gain_code_greenR**, **analogue_gain_code_red, analogue_gain_code_blue, analogue_gain_code_greenB)** and offset by offset control registers (**offset_gr, offset_r, offset_b, offset_gb**). Global analog gain can be set using analog gain con (**analogue_gain_code**).
the analog gain can be given by the following equation:

$$\text{Analog Gain} = (m_0 x + c_0) / (m_1 x + c_1)$$

S5K2E1FX03 specifies analog gain by coefficients of $m_0 = 0$, $c_0 = 128$, $m_1 = -1$, $c_1 = 128$. As a result, users can control analog gain as following equation:

$$\text{Analog Gain} = 128 / (128 - \textbf{analogue\_gain\_code [}15{:}0])$$

Separate channel gain is also supported in addition to global analog gain. Theoretically, maximum x128 gain can be obtained, but analog gain up to x8 is recommended for image quality.

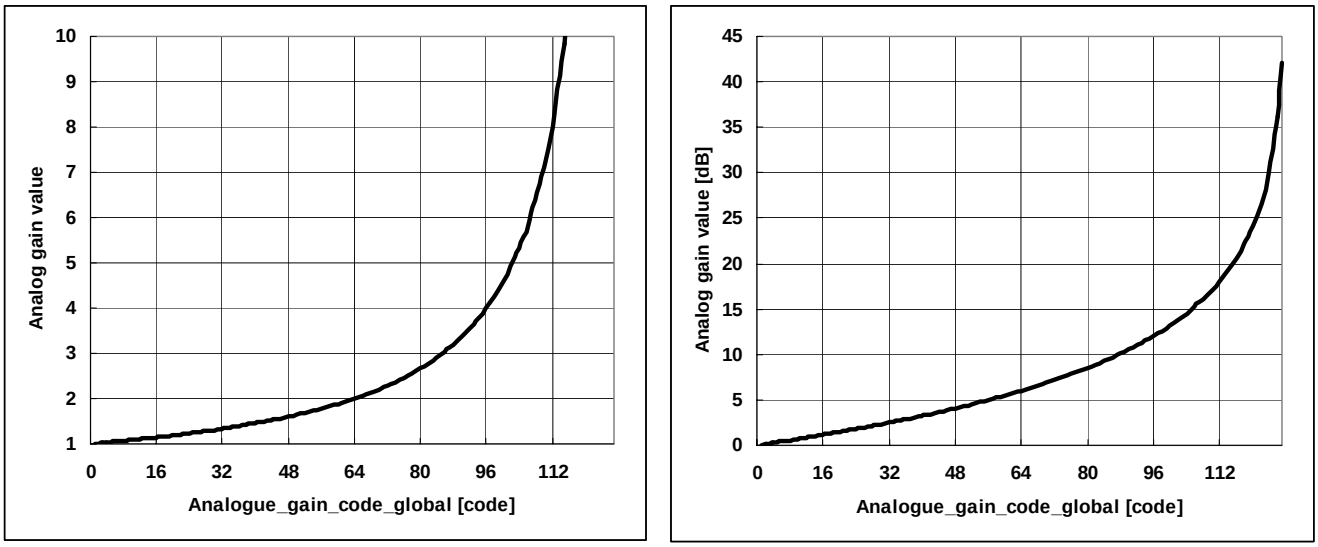


Figure 7: Analog Gain Value

2-3. Quadrisectional Global Gain Control

The user can controls the global gain to change the gain for all color channels by the Global Gain Control Registers (global_gain_sec1, global_gain_sed2, global_gain_sec3, global_gain_sec4). The global gain control

register is composed of four register groups and each register value decides the gain for each quarter section of output code level.
By appropriately programming these four register values, the different output resolution according to the signal can be achieved and the intra-scene dynamic range can be increased by 16 times. In another application, the sectional global gain control can be used as a rough gamma correction with four sectional linear approximation curve as shown in figure 7. (**ggs** is acronym of **global_gain_sec**)

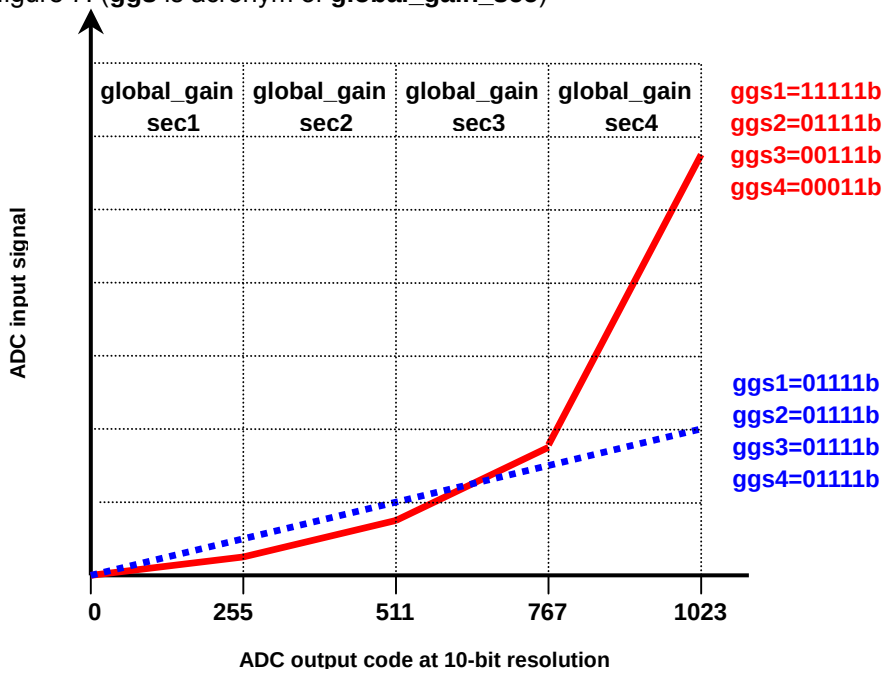


Figure 8: Quadrisectional Global Gain Control

3. POST PROCESSING

3-1. Dark Level Compensation

The dark level of Image sensor is defined as average output level without illumination. It includes pixel ouput caused by leakage current of the photodiodes and ADC offset. To compensate the dark level, the output level of optical black(OB) pixels can be a good reference value. When Auto Dark Level Compensation Register (**fadlc_en**) is set, the image sensor detects the OB pixel level at the start of every frame and anglog-to-digital conversion range is shifted to compensate the dark level for that frame. So, the resulting output data of that frame will be almost zero under dark state. If user wants the dark level which is not zero, the ADC Offset Register (**even_cnt_del**, **odd_cnt_del**) can be used. The lower 7-bit value represent the offset value in outout code for compensation and the MSB is the sign to define whether the offset is positive (**even_cnt_del**[7], **odd_cnt_del**[7]=0) or negative(**even_cnt_del**[7], **odd_cnt_del**[7]=1). When not in auto dark level compensation mode, the **even_cnt_del**[7:0], **odd_cnt_del**[7:0] act as a output code value to subtract the output image data. Please notify that the all the 8-bit data are used for an offset value without sign bit.

ADLC formula : Dfinal = D(n) + **even_cnt_del**[7:0] (**odd_cnt_del**[7:0])
D(n) = (gain_a)*(OB(n) + OB(n-1)) + (gain_b)*D(n-1)

3-2. Scaler

The image scaling function within the sensor module provides a flexible way of generating lower resolution full

field of view image data, at a reduced data rates, for viewfinder and video applications. The scaler is able to scale the full resolution of the sensor module down to within 10% of the target image size (the smallest output size is 256x192). This flexibility means that sensor modules can support a wide range of LCD viewfinder sizes and different codec resolutions

To provide a wider range of data rate reduction options the full image scaler is able to reduce the data rates in both the horizontal and vertical directions. This is achieved by the use of a FIFO between video timing and output clock domains (Figure 18).

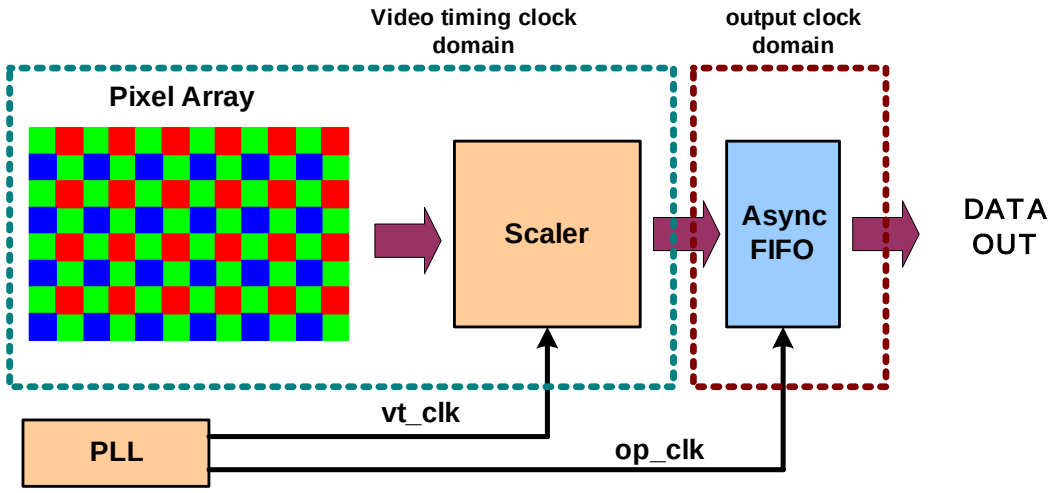


Figure 9: Full Scaler Block Diagram

Clock divider setting restrictions are as follows when scaling mode is on:

$$1 \le \frac{op\_sys\_div \times op\_pix\_div}{vt\_sys\_div \times vt\_pix\_div} \le \left(\frac{scale\_m}{scale\_n}\right)^2$$, for full scale down

$$1 \le \frac{op\_sys\_div \times op\_pix\_div}{vt\_sys\_div \times vt\_pix\_div} \le \left(\frac{scale\_m}{scale\_n}\right)$$, for horizontal scaling only

For the proper scaler operation, the **fifo_threshold** register value should be specified according to the scale_m as described below :

fifo_threshold = H_valid x clk_factor – H_scale + line_off + 10 , for scale_m < 32
where H_valid is the valid sensor data numbers,
clk_factor = vt_pix_div x vt_sys_div / (op_sys_div x op_pix_div),
H_scale = H_valid x scale_n / scale_m,
line_off = [line_length_pck x scale_m / scale_n x clk_factor]fraction_part x V_scale,
V_scale = V_valid x scale_n / scale_m, and decimal 10 is the marginal number.
fifo_threshold = H_valid x scale_n / scale_m + 20 , for scale_m >= 32
where scale_n is fixed to decimal 16.

For example, when 'H_valid is 2620, V_valid is 1968, clk_factor is 1, line_length_pck is 3176 and scale_m is 20', fifo_water_mark_pixels becomes 534 (2620 x 1 - 2096 + 0 + 10 ≈ 524).

The procedure of scaler setting is described below :

1) **scale_m** decision considering the scale-downed target image :
(The scale-downed image size must be greater or equal than target image size.)
Ex) If scale_m = 20 and original image size = 2620 x 1968,
then scale-downed image size becomes 2620x1968/(20/16) = 2096 x 1574 in ideal.
But the scale-downed image size is roughly 2092x1570(minus 4) in real.

2) clock factor decision :

$$1 \le \frac{op\_sys\_div \times op\_pix\_div}{vt\_sys\_div \times vt\_pix\_div} \le \left(\frac{scale\_m}{scale\_n}\right)^2$$, for full scale down

$$1 \le \frac{op\_sys\_div \times op\_pix\_div}{vt\_sys\_div \times vt\_pix\_div} \le \left(\frac{scale\_m}{scale\_n}\right)$$, for horizontal scaling only

3) Using the 1), 2) results, calculate the **fifo_threshold** :

4. I²C SERIAL INTERFACE

4-1. IIC Bus Overview

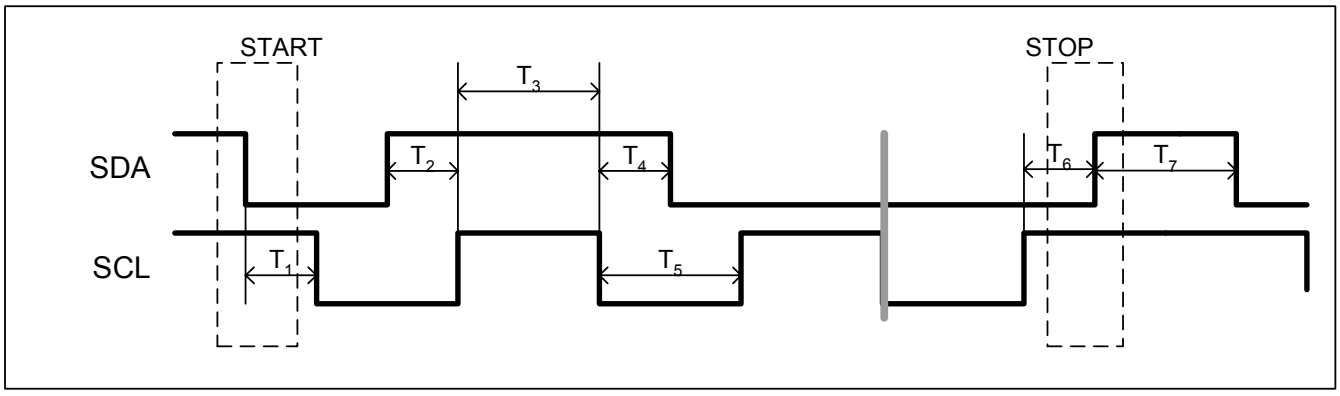
The IIC contains a serial two-wire (half duplex) interface that features bi-directional operation, master or slave mode. The general SDA and SCL are the bi-directional data and clock pins, respectively. These pins are open-drain type ports and will require a pull-up resistor to VDD. The SDA bus line may only be changed while SCL is low. The data on the SDA bus line is valid on the high-to-low transition of SCL.

4-2. Protocol

The IIC bus interface is composed of following parts. START signal, 7-bit slave device address (0101101b) transmission followed by a read/write bit, an acknowledgement signal from the slave, 8-bit data transfer followed by an acknowledgement signal and STOP signal.

4-3. Notice & Usage

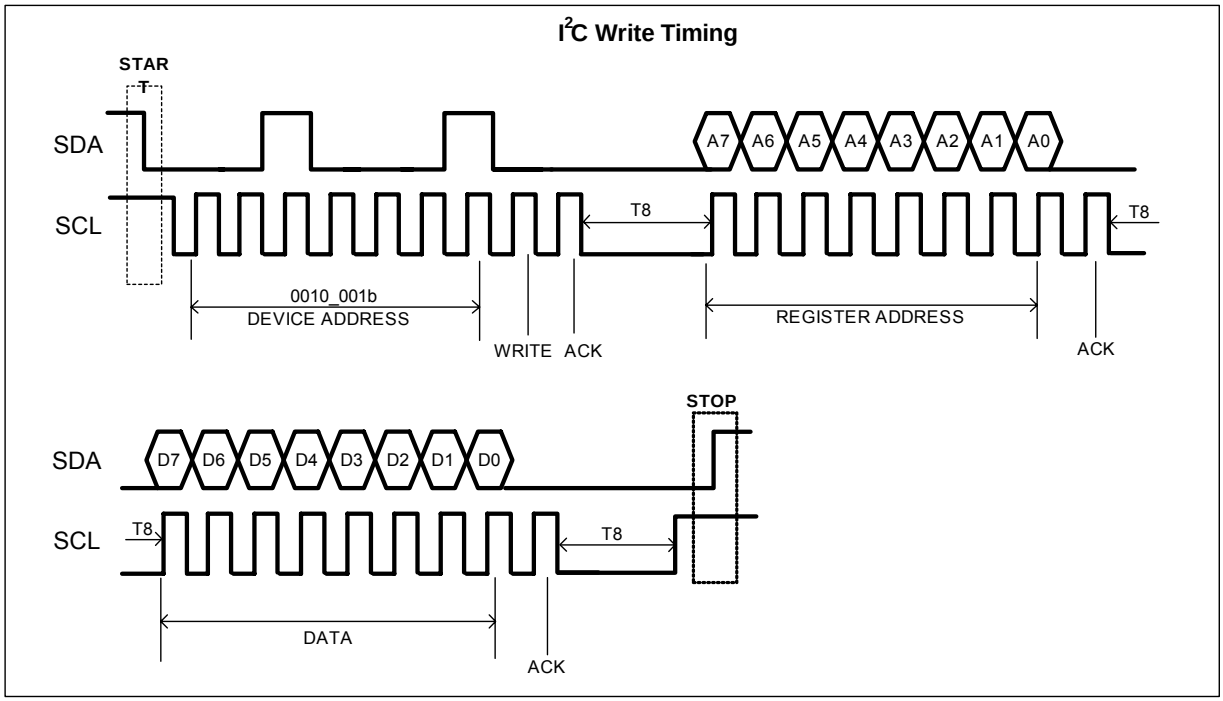
The S5K2E1FX03 internal registers have several pages to expand its address space. Our host interface uses only 8-bit data to assign a register, thus a page setting must be required in advance and its selected page will be kept until changed.



SYMBOL	PARAMETER	MIN	MAX	UNIT
	SCL clock frequency	-	400	KHz
T1	Hold time for START condition	0.6	-	us

T2	Data setup time	100	-	ns
T3	High period of the SCL clock	0.6	-	us
T4	Data hold time	10	-	ns
T5	Low period of the SCL clock	1.3	-	us
T6	Setup time for STOP condition	0.6	-	us
T7	Bus free time between a STOP and START condition	1.3	-	us

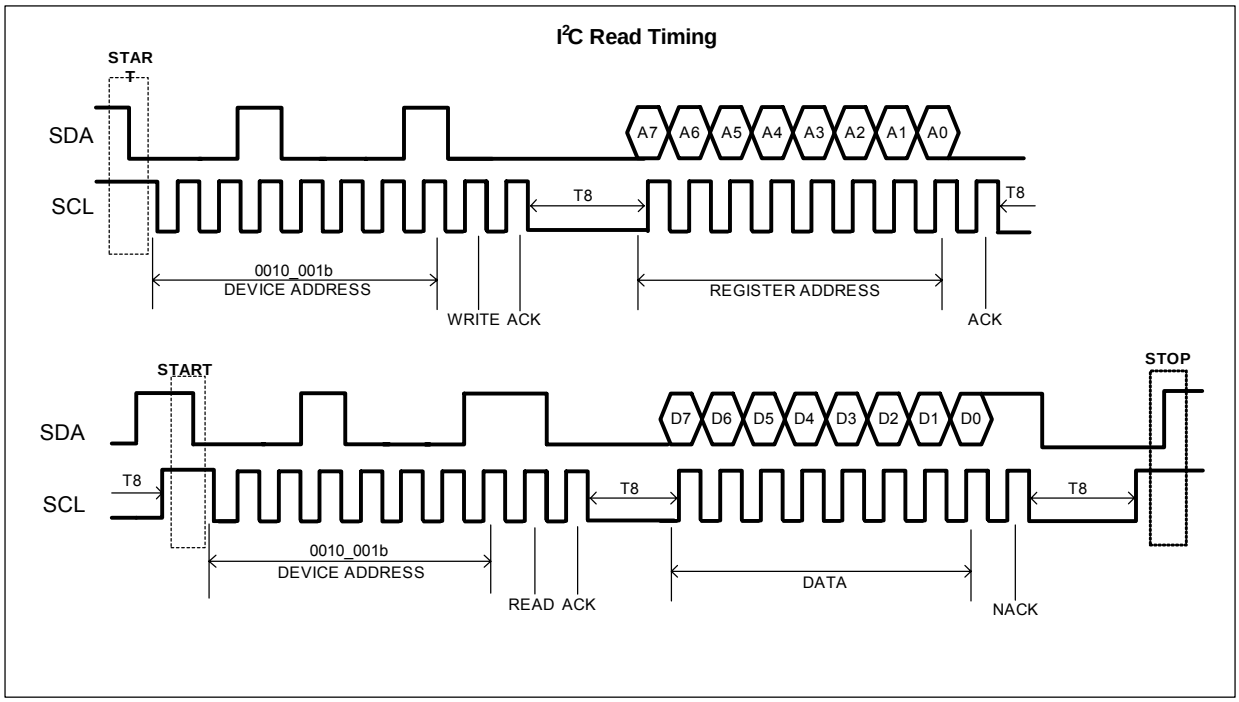
Figure 10: IIC General Timing



SYMBOL	PARAMETER	MIN	MAX	UNIT
T8	Minimum required time for slave Interrupt processing	150	-	cycle

[NOTE]
(1) cycle: MCLK cycle time

Figure 11: IIC Write Timing



SYMBOL	PARAMETER	MIN	MAX	UNIT
T8	Minimum required time for slave Interrupt processing	150	-	cycle

[NOTE]
(1) cycle: MCLK cycle time
(2) A repeated START is required

Figure 12: IIC Read Timing

5. PLL and Clock Generator

S5K2E1FX03 contains a Phase-Locked Loop(PLL) and a clock generator, which generates all the necessary video timing and output pixel clocks from the external clock of 6 ~ 27MHz. By setting pre PLL clock divider(**pll_p**), PLL multiplier(**pll_m**) and clock dividers(**dck_div1&2, pck_div1&2**) appropriately, users can get necessary clock frequency.
The overall clock tree structure is shown in Figure 11, and there are shown user-controllable divide-ratios.
The necessary frequencies are synthesized by the following equations.

PLL input clock = external input clock / pre PLL clock divider
PLL output clock = PLL input clock * PLL multiplier
Data clock (DCK) = PLL output clock / (DCK clock divider 1 * DCK clock divider 2)
Pixel clock (PCK) = PLL output clock / (PCK clock divider 1 * PCK clock divider 2)

Using the external clock frequency of 13 MHz and default register setting, the data and pixel clock frequency is 32.5MHz.

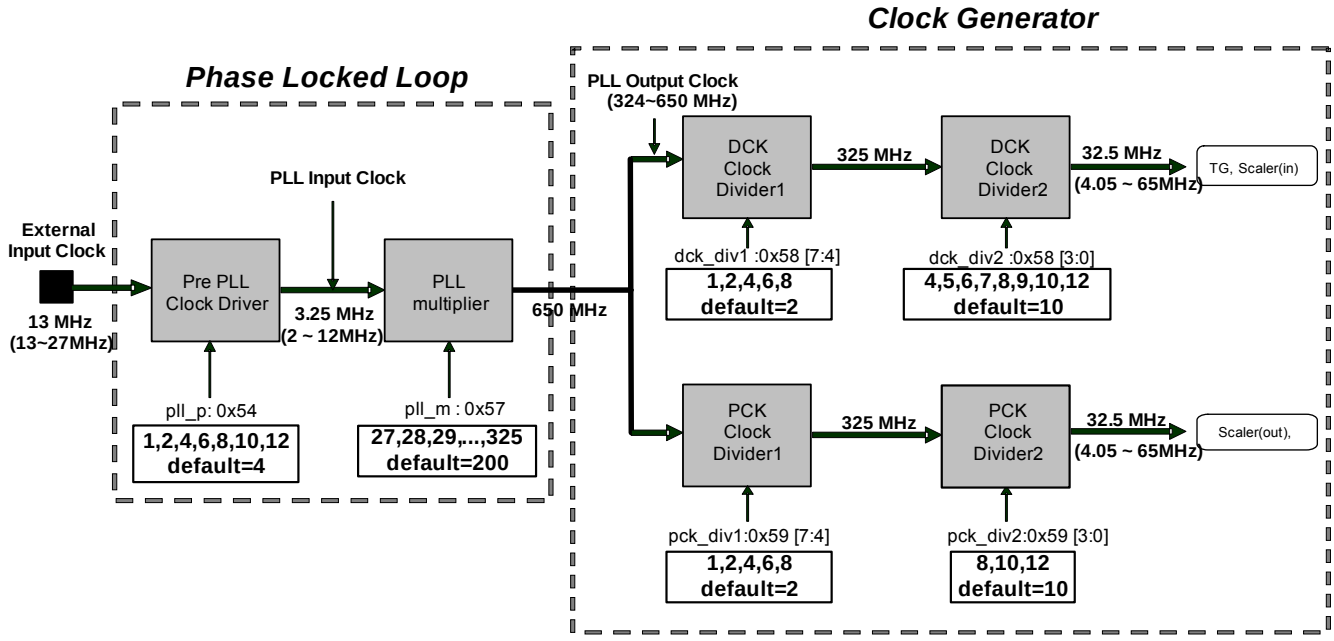


Figure 13: Clock tree structure

SYNC CONTROL AND TIMING DIAGRAM

SYNC CONTROL

Table 3: Sync Control mode

Case	func0_sel	sync_mode	scale_mode	Output sync
1	0	0	00/01/10/11	Scaler data out Data valid sync
2	1	1	x	TG data out 1. Data valid sync (When vs_disp=1'b1, hs_disp=1'b1) 2. Controllable sync (When vs_disp=1'b0, hs_disp=1'b1)

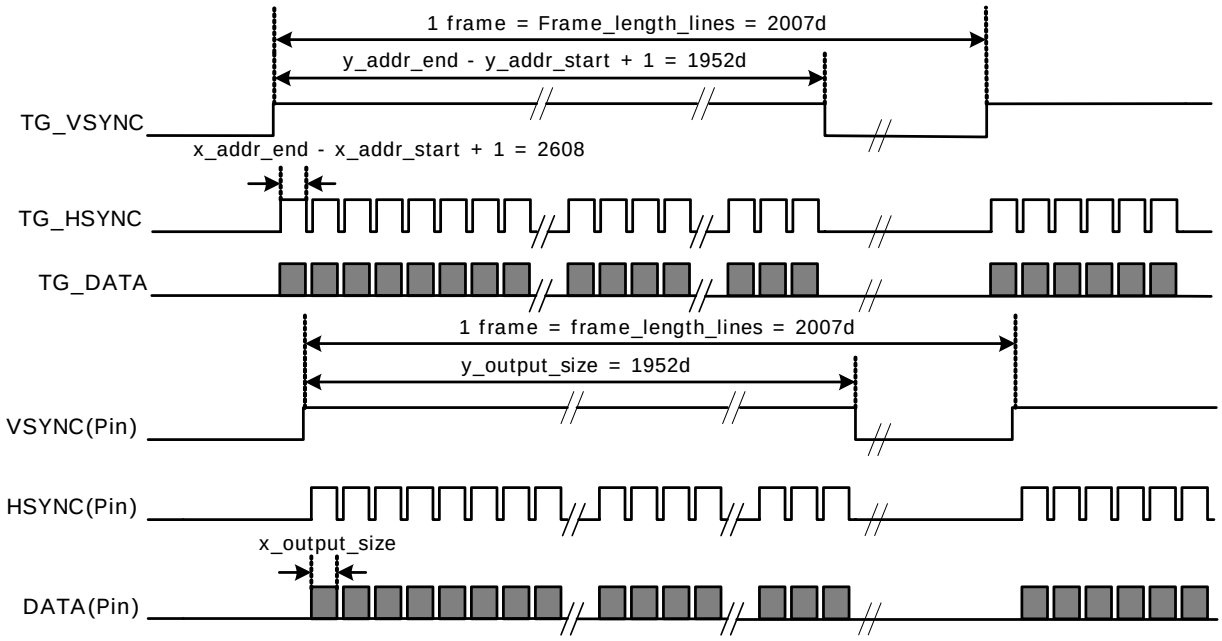
[Notes:]
(1) Above table is base on data-valid-mode. Case 2 also can be controlled by other mode.
(2) vs_disp, hs_disp needs to be regulated under circumstances.

1. Continuous Frame Capture Mode

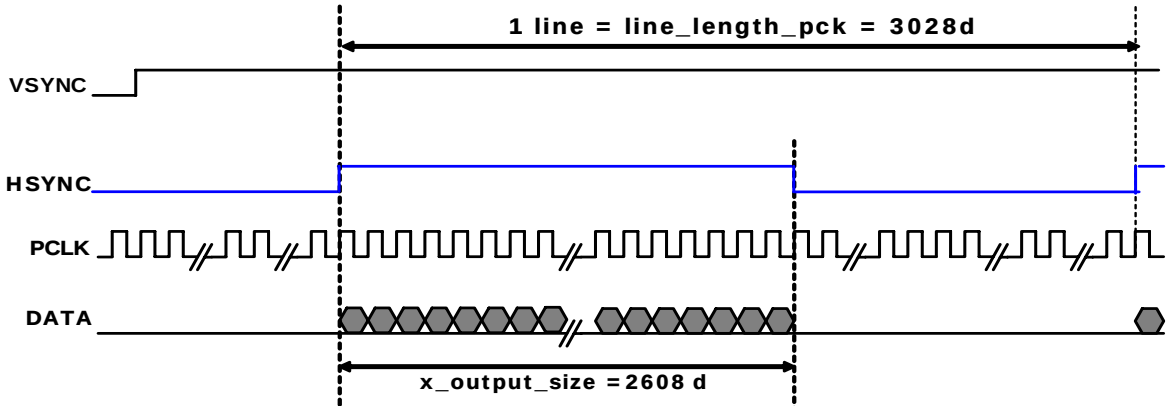
Case1. Data valid mode

- func_sel = 1'b0, sync_mode = 1'b0, scale_mode = 2'b00/01/10/11
- Data valid sync

Vertical Timing Diagram



Horizontal Timing Diagram

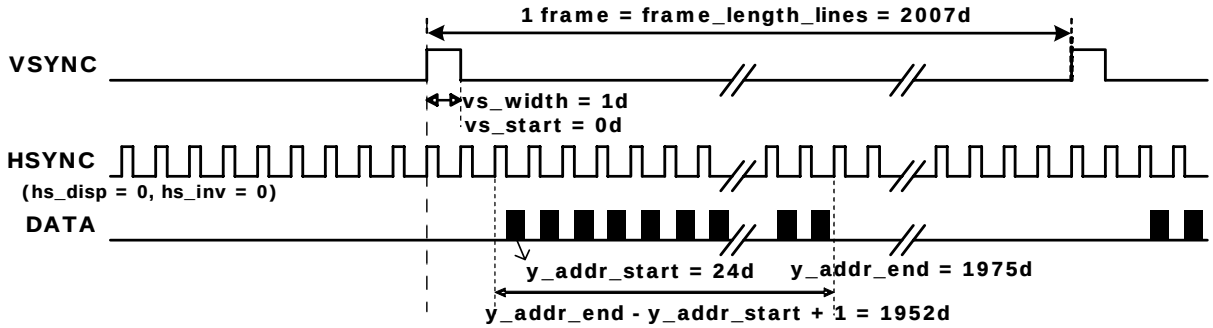


Case2. Special Case

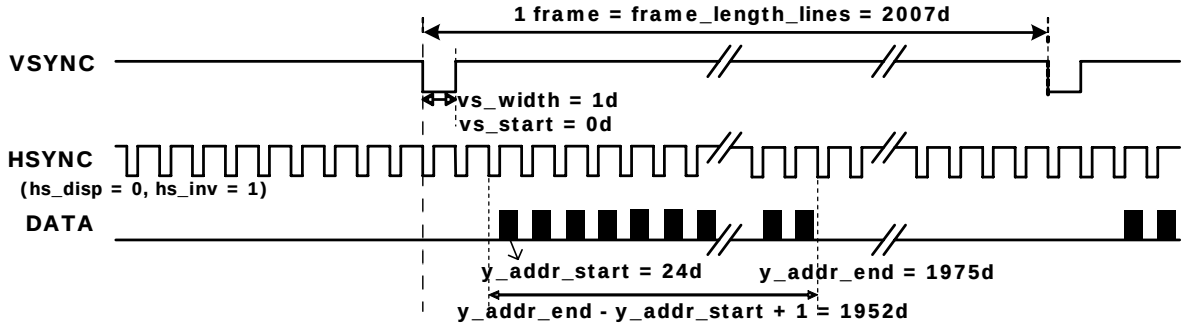
- No use Scaler, func_sel = 1'b1
- Sensor output data direct readout case

Vertical Timing Diagram

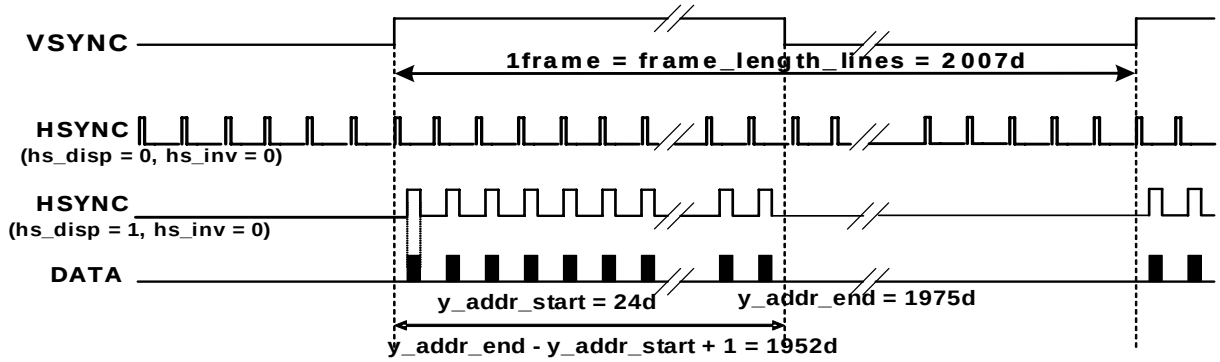
1) Default mode (vs_disp = 1'b0, vs_inv = 1'b0)



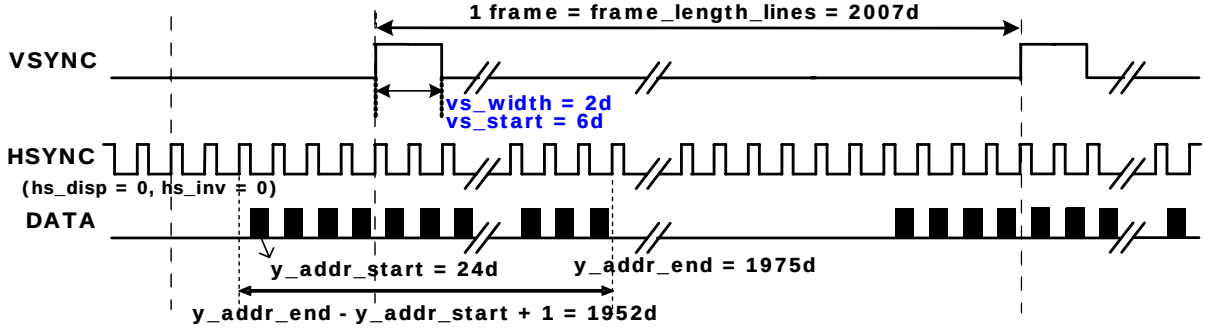
2) Sync polarity inversion mode (vs_disp = 1'b0, vs_inv = 1'b1)



3) Vertical data valid mode (vs_disp = 1'b1, vs_inv = 1'b0)

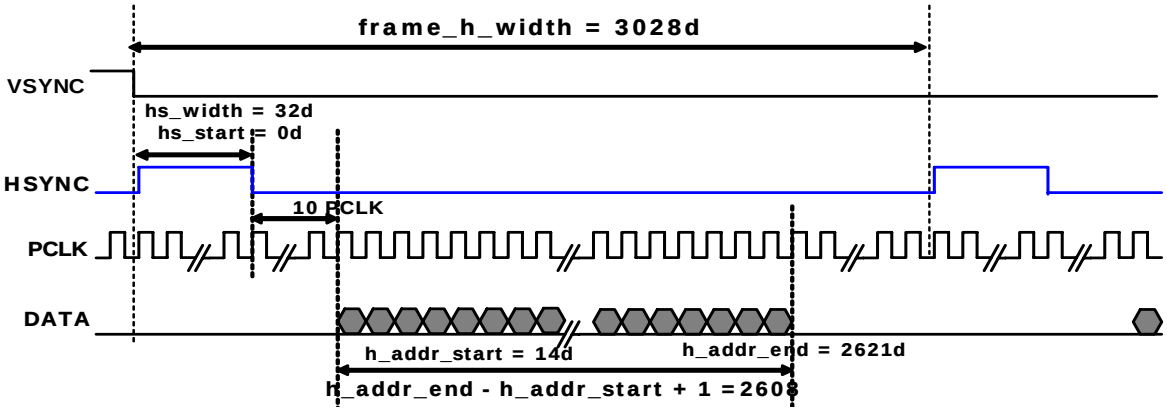


4) Delayed vertical sync mode : vs_start, vs_width (ex) vs_start = 6, vs_width = 2)

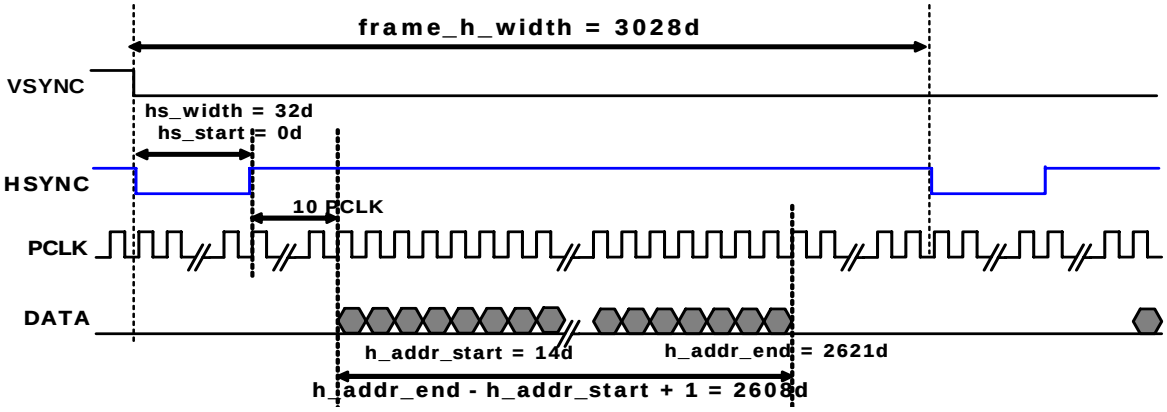


Horizontal Timing Diagram

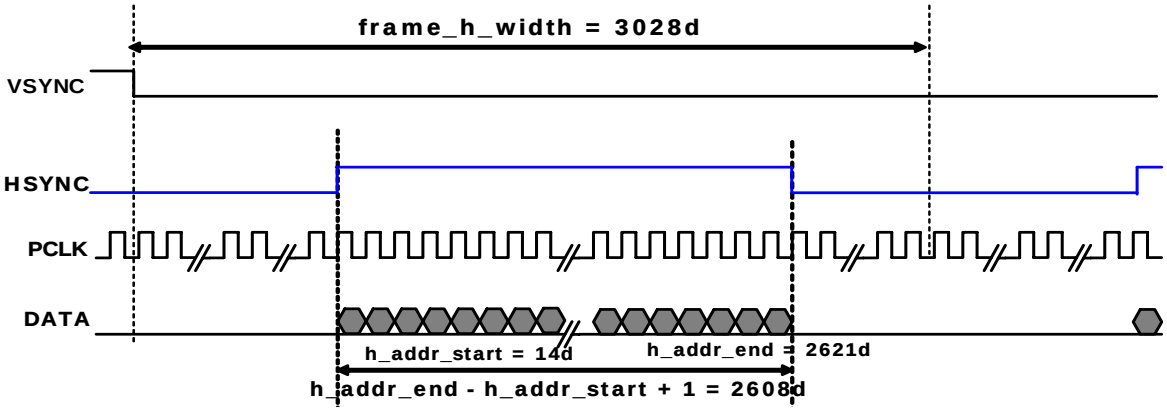
1) Default mode (hs_disp = 1'b0, hs_inv = 1'b0)



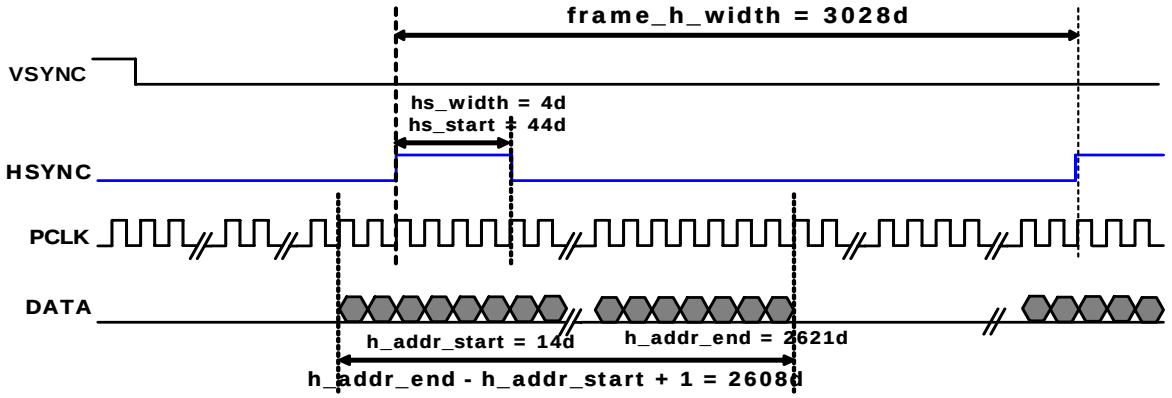
2) Sync polarity inversion mode (hs_disp = 1'b0, hs_inv = 1'b1)



3) Horizontal data valid mode (hs_disp = 1'b1, hs_inv = 1'b0)

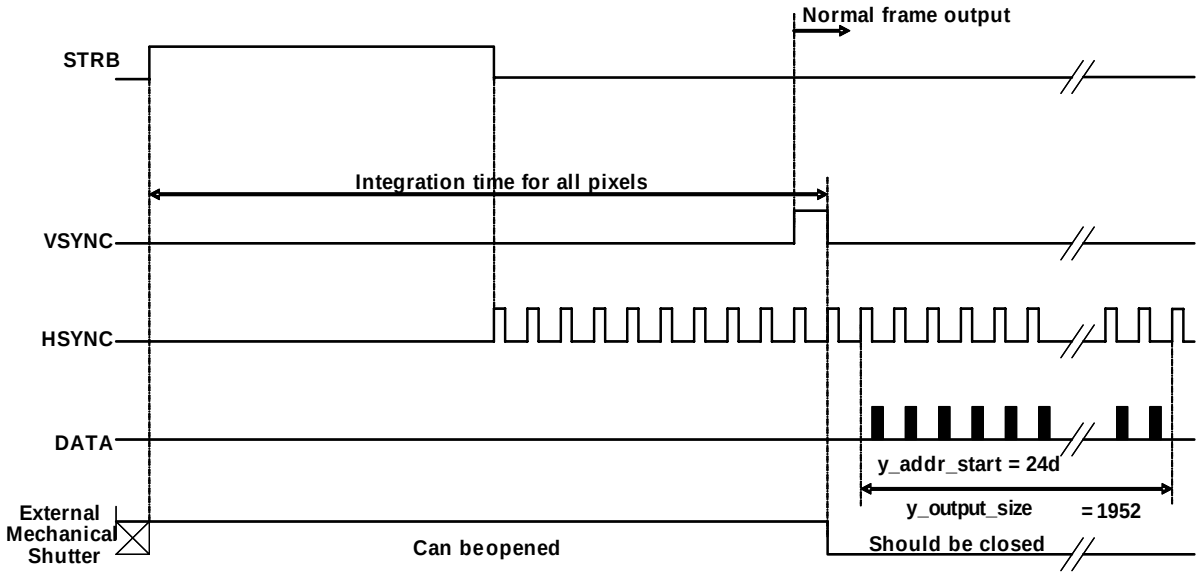


4) Delayed horizontal sync mode : hs_start, hs_width (ex) hs_start = 44, hs_width = 4)



2. Single Frame Capture Mode

1) Mechanical Shutter Case : sfcm_en=1 & mech_mod = 1



REGISTER UPDATE TIMING

Gain and Shutter register is not applied at same time sequentially. Gain register is applied right after next frame but Shutter register needs one more frame time.

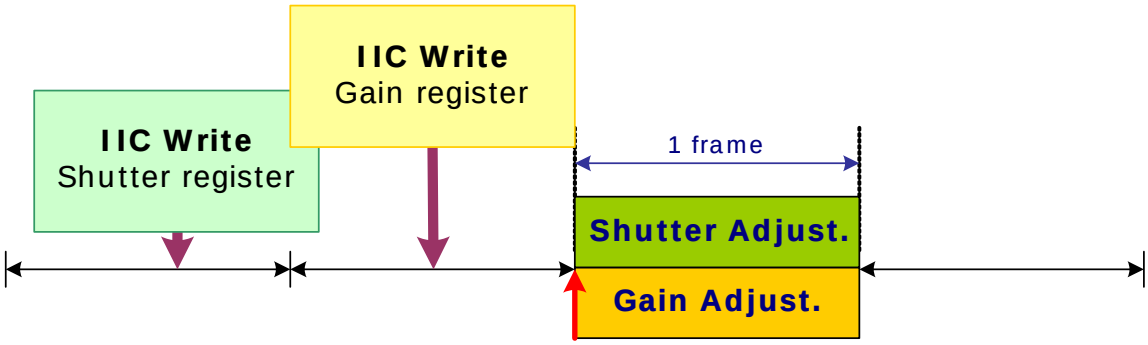


Figure 14: Register Update Timing

IMAGE CAPTURE SYSTEM

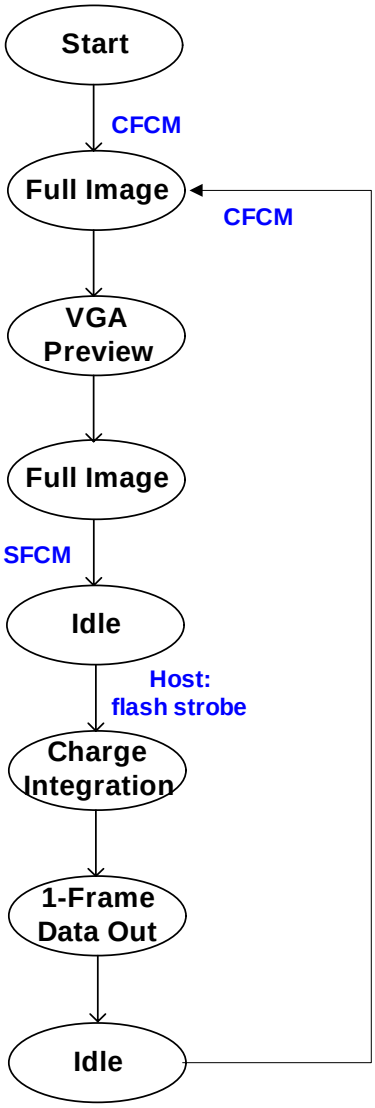


Figure 15: Block Diagram of Image Capture System

VGA PREVIEW USING SUBSAMPLING

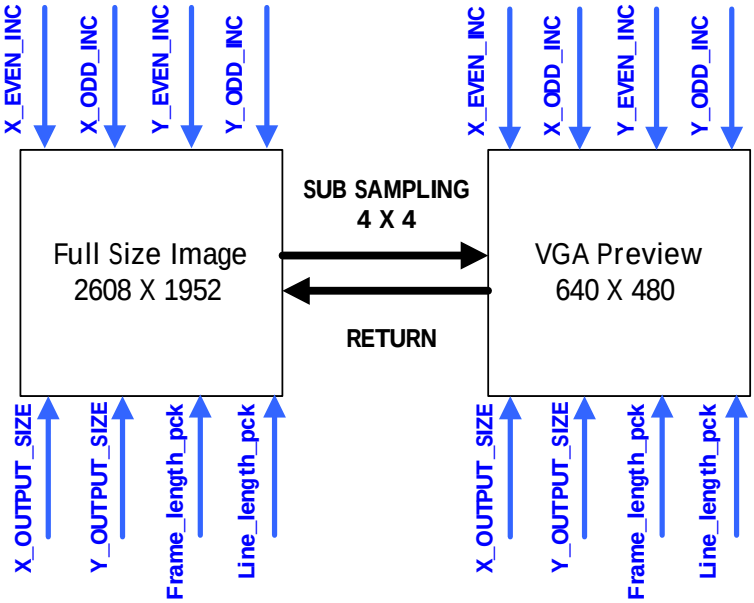


Figure 16: Size Setup Using Subsampling

Table 4: Sub sampling Register

NAME	REGISTER	DESCRIPTION	Register Value Full Image	Register Value VGA Preview
X_OUTPUT_SIZE	0x2c~2d	Horizontal output size	0x0ac0	0x0280
Y_OUTPUT_SIZE	0x2e~2f	Vertical output size	0x07a0	0x01e0
X_EVEN_INC	0x30	Increment in x direction for even pixels - 0, 2, 4, etc.	0x01	0x01
X_ODD_INC	0x31	Increment in x direction for odd pixels - 1, 3, 5, etc.	0x01	0x07
Y_EVEN_INC	0x32	Increment in y direction for even pixels - 0, 2, 4, etc.	0x01	0x01
Y_ODD_INC	0x33	Increment in y direction for odd pixels -1, 3, 5, etc.	0x01	0x07
Frame_length_pck	0x20~21	Length of frame in unit of line length minimum blanking lines is 12d.	0x07d8	0x028c
Line_length_pck	0x22~23	Length of line in unit of data clock	0x0c68	0x0c68
Global gain global	0x16	Global gain	12h	09h
Avg_sub_smp_en	0x0e[0]	Average sub_sampling_enable	0b	1b
S1r_end_val	0x4d[7:4]	0h for avg.subsampling	fh	0h
S3_end_val	0x4e[3:0]	fh for avg.subsampling	0h	fh

VGA PREVIEW USING SCALER

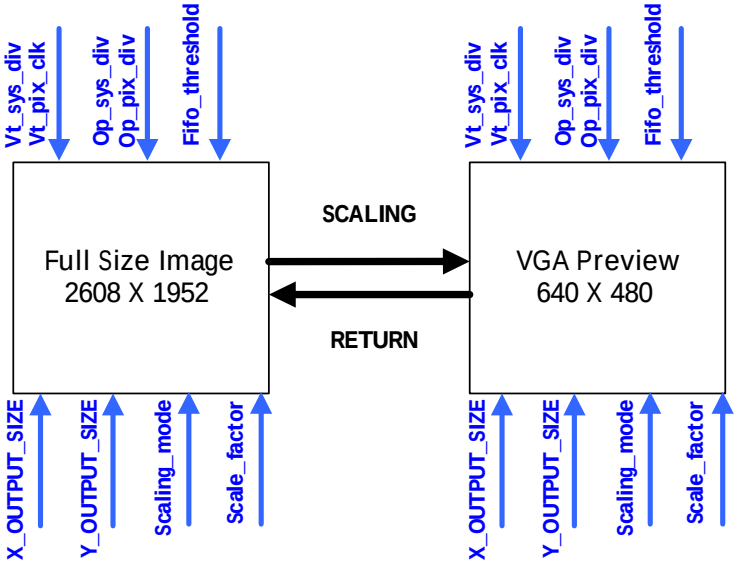


Figure 17: Size Setup Using Scaler

Table 5: Scaling Register

NAME	REGISTER	DESCRIPTION	Register Value Full Image	Register Value VGA Preview
X_OUTPUT_SIZE	0x2c~2d	Horizontal output size	0x0ac0	0x0280
Y_OUTPUT_SIZE	0x2e~2f	Vertical output size	0x07a0	0x01e0
Scaling_mode	0x60	0 – No scaling 1 – Horizontal Scaling 2 – Full Scaling	0x00	0x02
Scale_factor	0x61	Down scale factor: M component Range: 16 to upwards , Max : 0xA4	0x10	0x40
Fifo_threshold	0x64~65	Threshold level that scaler start to transmit the scaled image when scaling is used. Units : pixels	0x0a40	0x02a3
Vt_sys_div	0x58 [7:4]	Data clock divider 1 control	0x2	0x2
Vt_pix_div	0x58 [3:0]	Data clock divider 2 control	0xa	0xa
Op_sys_div	0x59 [7:4]	Pixel clock divider 1 control	0x2	0x2
Op_pix_div	0x59 [3:0]	Pixel clock divider 2 control	0xa	0xa

[NOTE]

fifo_threshold = H_valid x scale_n / scale_m + 20 = 0x02a3

where scale_m = 64d, scale_n is fixed to 16d, H_valid is 2620d.

MECHANICAL SHUTTER OPERATION

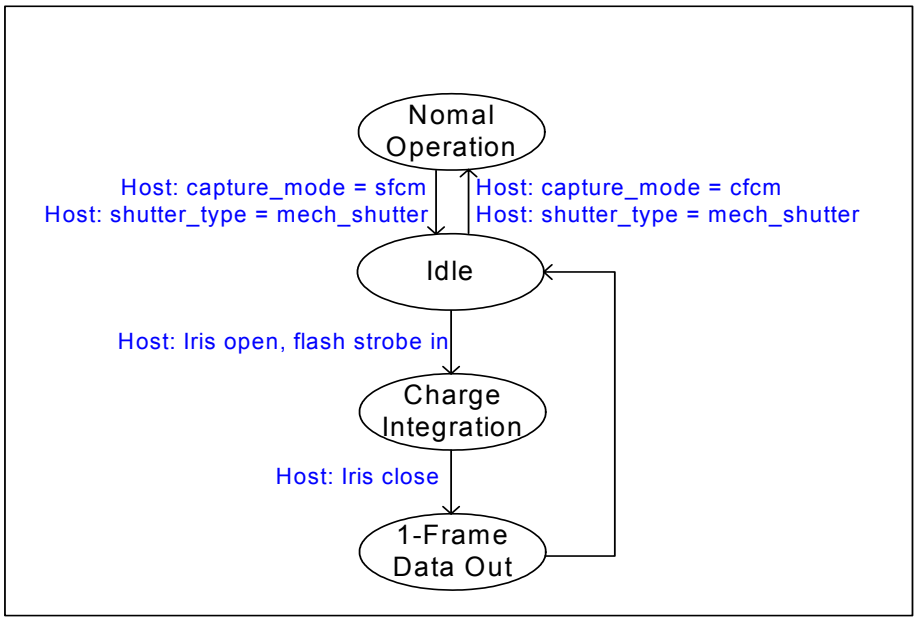


Figure 18: Mechanical Shutter Operation Scenario

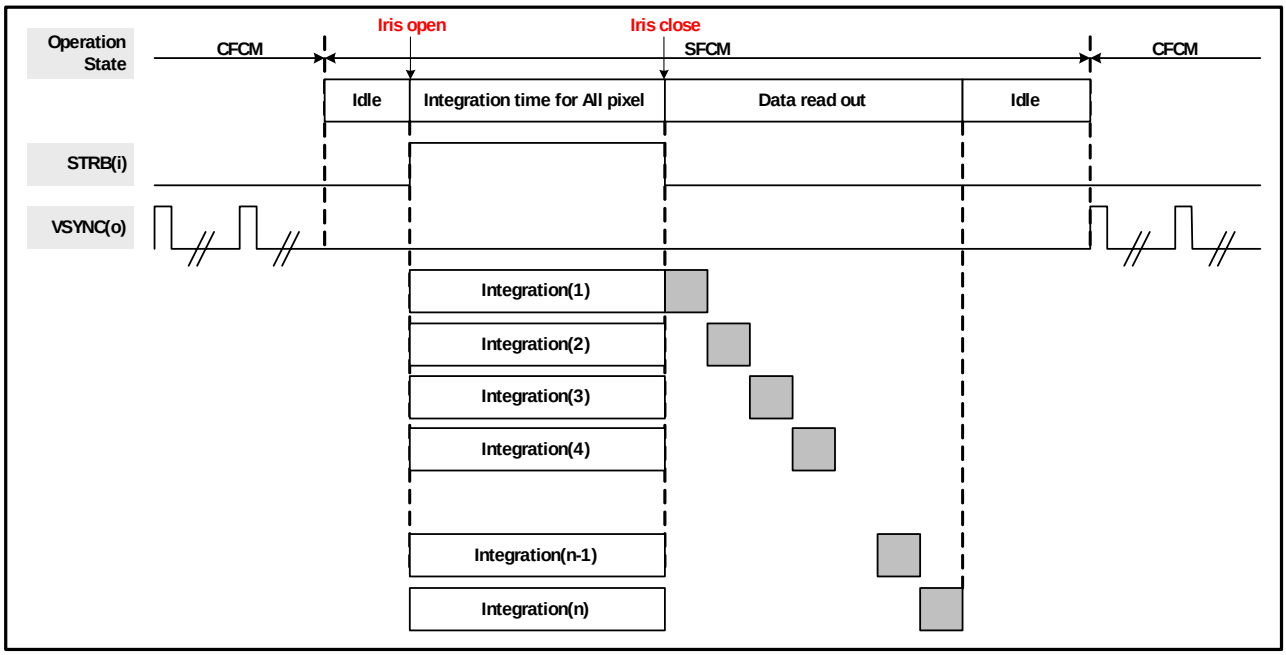


Figure 19: SFCM Operation Timing with Mechanical shutter

POWER UP/DOWN SEQUENCE

The digital and analog supply voltages can be powered up in any order e.g. VDDD then VDDA or VDDA then VDDD.

On power up :

- If STBYN is low when the power supplies are brought up then the sensor will go into power-down mode.
- If STBYN is high when the power supplies are brought up then the sensor will go into software stand-by mode

In both cases the presence of an on-chip power-on reset cell ensures that the internal register values are initialized correctly to their default values. The MCLK clock can either be initially low and then enabled during stand-by mode or MCLK can be a free running clock.

As shown in Figure 12, the operation state is composed of 3 modes which are power-down, stand-by and active operation modes.
During the power-down mode where external power supplies are applied and STBYN is in low state, sensor does not operate and the current consumption of power supplies are nearly zero. In this operation mode, all I^2C registers are reset to their defaults values. During the stand-by mode where STBYN is switched to high state, the current consumption of power supplies are minimized and I^2C communication is possible. The clock divider and PLL multiplier registers must be configured during stand-by mode while PLL is powered down. Sensor enters active operation mode by setting **streaming** register (Bit[4] of Reg0x03h) to 1b where pixel data is output through D10 ~ D0 pins.

The power down sequence is the reverse order of power up sequence, i.e., active operation mode → stand-by mode → power down mode.

Table 6: Power-Up Sequence Timing Constraints

Constant	Label	Min	Max	Units
VDDA rising – VDDD rising	t0	VDDA and VDDD may rise in any order. The rising separation can vary from 0ns to indefinite		ns
VDDD rising – VDDA rising	t1			ns
VDDA rising – STBYN rising	t2	0.0		ns
STBYN rising – First I^2C transaction	t3	15us + 16 MCLK Cycles		
Minimum No. of MCLK cycles prior to the first I2C transaction	t4	16		MCLK cycles

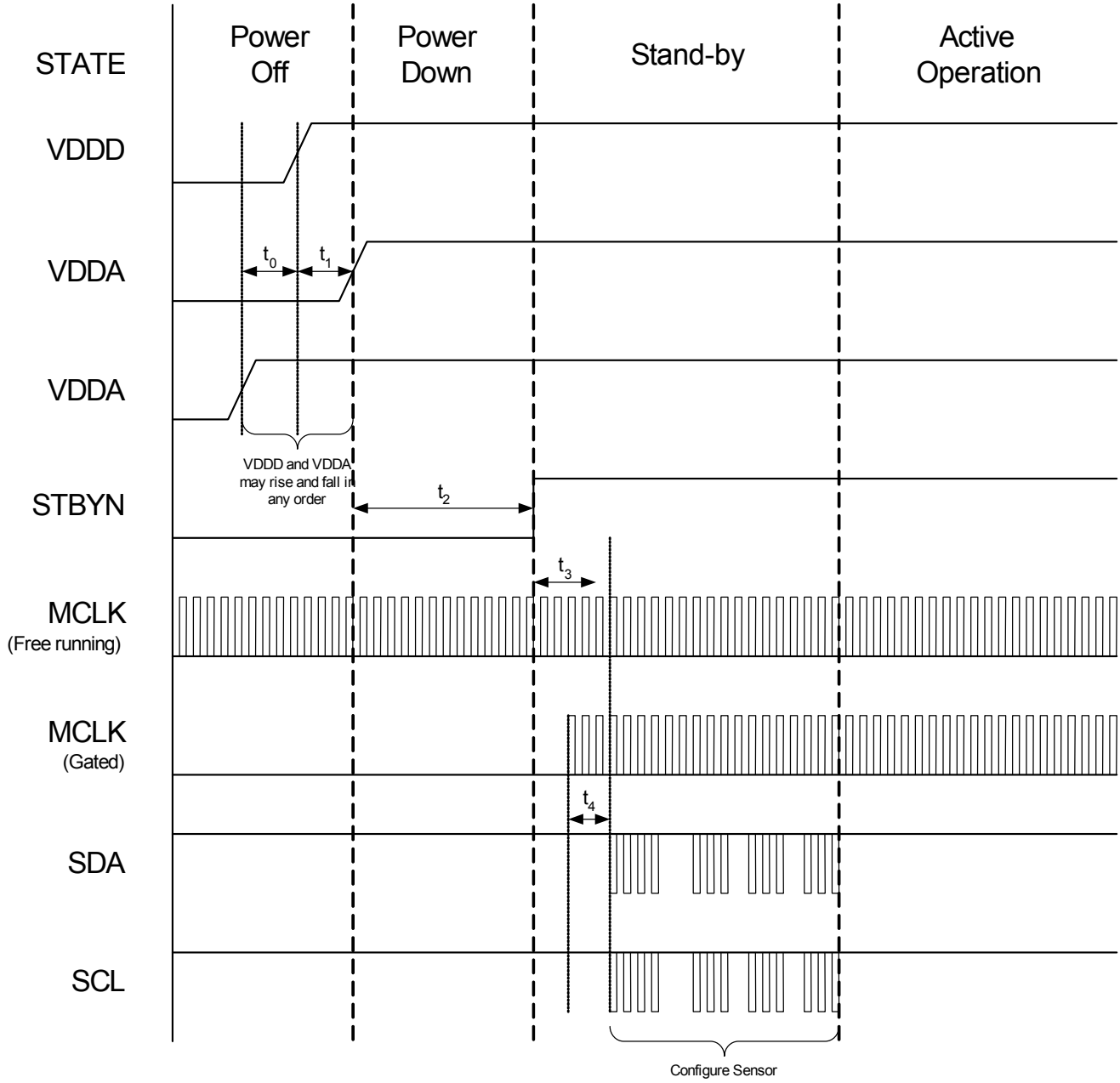


Figure 20: Power-Up Sequence

ELECTRICAL CHARACTERISTICS

Table 7: Absolute Maximum Rating

Symbol	Description	Min	Typical	Max	Units
VDDD	Digital Absolute Max (1)	-0.3		2.2	V
VDDA	Analogue Absolute Max (2)	-0.3		4	V
$V_{IP(DIG)}$	Digital Input Voltages (3)	-0.3		VDDA+0.3	V
T_{STR}	Storage Temperature	-40		85	°C

[Notes:]
(1) Digital Supply 1.9V + 0.3V
(2) Analogue Supply 2.9V + 0.3V
(3) Digital Inputs: MCLK, STBYN, SCL, SDA, SCE, TST0, TST1, TST2

Table 8: DC Characteristics

(T_A = -30 to +70°C, C_L = 15pF)

Characteristics	Symbol	Condition	Min	Typ	Max	Unit
Operating voltage	V_{DDH}	applied to VDDA pins	2.4	2.8	2.9	V
	V_{DDL}	applied to VDDD pin	1.7	1.8	1.9	
Input voltage(1)	V_{IH}	-	0.975	-	2.8	
	V_{IL}	-	-0.3	-	0.525	
Input leakage current(2)	I_{IL}	$V_{IN} = V_{DDL}$	-10	-	10	μA
Input leakage current with pull-down(3)	I_{ILD}	$V_{IN} = V_{DDL}$	10	20	44	
High level output voltage(4)	V_{OH}	I_{OH} = -1μA	V_{DDL}-0.05	-	-	V
		I_{OH} = -4mA	1.125	-	-	
Low level output voltage(5)	V_{OL}	I_{OL} = 1μA	-	-	0.05	
		I_{OL} = 4mA	-	-	0.375	
High-Z output leakage current(6)	I_{OZ}	$V_{OUT} = V_{SS}$ or V_{DDL}	-10	-	10	μA
Input capacitance(1)	C_{IN}	-	-	-	4	pF
Supply current	I_{STBL}	STBYN=Low(Active) All input clocks = Low 0 lux illumination applied to VDDD pin	-	-	10	μA
	I_{STBH}	STBYN=Low(Active) All input clocks = Low 0 lux illumination applied to VDDA pin	-	-	10	μA
	I_{DDL}	f_{DCLK} = 32.5MHz 0 lux illumination applied to VDDD pin	-	TBD	TBD	mA
	I_{DDH}	f_{DCLK} = 32.5MHz 0 lux illumination applied to VDDA pin	-	TBD	TBD	mA

NOTES:

1. Applied to MCLK, STBYN, SCL, SDA, SCE, TST0, TST1, TST2 pins.
2. Applied to MCLK, STBYN, SCL, SDA, TST0, TST1, TST2 pins
3. Applied to SCE pin
4. Applied to DCLK, HSYNC, VSYNC, D0 to D10 pin. I_{OH} : High level output current
5. Applied to DCLK, HSYNC, VSYNC, D0 to D10, SCL, SDA pin. I_{OL} : Low level output current
6. Applied to SDA, HSYNC, VSYNC, D0 to D10 pin when in High-Z output state

Table 9: Imaging Characteristics

(All the values are obtained by using the SMIA 1.0 characterization method. Electrical operating conditions follow the recommended typical values. The control registers are set to the default values. T_A = 25°C if not specified.)

Characteristics	Min	Typ	Max	Unit
Sensitivity		2		1/lux.sec
Photo response non - uniformity		1.38	2	%
SNR at 0.1lux		23		dB
SNR at 1 lux		33		dB
SNR at 10 lux		39		dB
SNR at 100 lux		39		dB
Maximum illumination		100000		Lux
Minimum illumination		0.01		Lux
VFPN Level		0.00018		-
VFPN Max		0.00052		-
HFPN Level		0.0021		-
HFPN Max		0.0014		-
Temporal Noise		-57.5		dB
Column Noise Level		-86.8		dB
Column Noise Max		-81.2		dB
Row Noise Level		-72.7		dB
Row Noise Max		-70.8		dB
Dark Signal		0.00033	0.001	1/sec
Dark Signal Non-Uniformity		0.0074	0.0147	1/sec
Image Lag		0.001	0.003	-

Table 10: AC Characteristics

(V_{DDH} = 2.8V, V_{DDL} = 1.8V ± 0.1V, T_A = -30 to + 70 °C, C_L = 10pF)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
Main input clock frequency	f_{MCLK}	Duty = 50%	6	13	27	MHz
Data output clock frequency	f_{DCLK}	-	4.05	32.5	65	
Propagation delay time from data output clock	t_{PDDV}	VSYNC output	-	-	TBD	
	t_{PDDH}	HSYNC output	-	-	TBD	
	t_{PDDO}	DATA output	-	-	TBD	
STBYN input pulse width	t_{WSHB}	STBYN=low(active)	TBD	-	-	

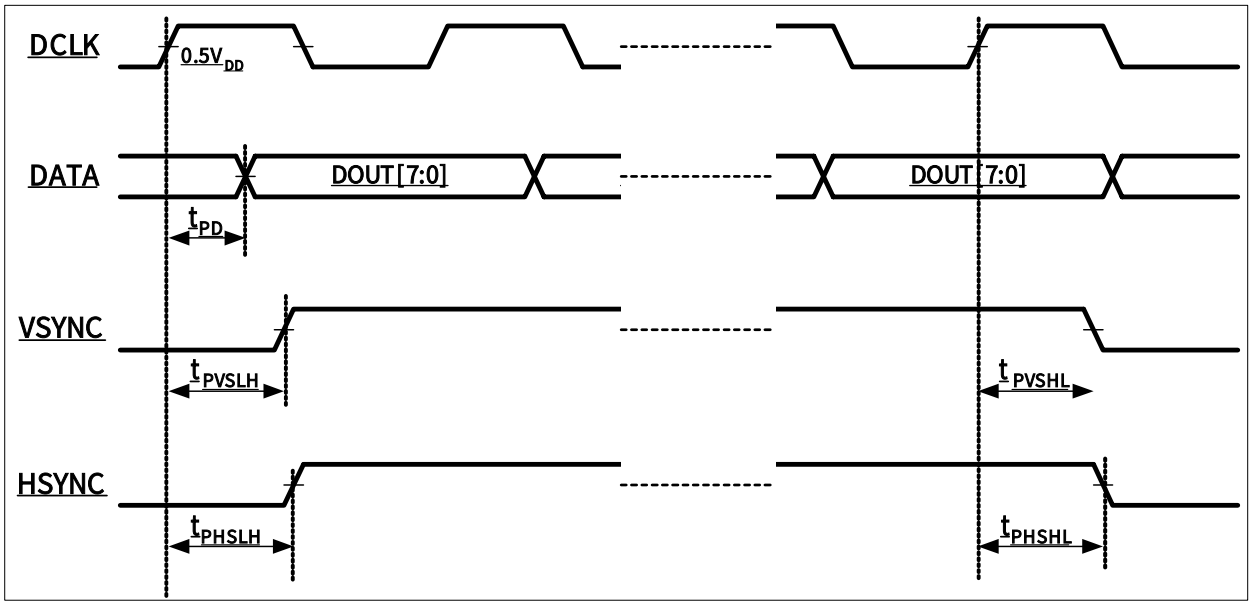


Figure 21: Propagation Delays for DCLK, Data Out, VSYNC, and HSYNC

Table 11: Electrostatic Characteristics

INDEX	Electrostatic Standard			UNIT	Remark
	PIN NO.	Design Target	Reference Product		
Human Body Model	ALL	TBD		V	
Machine Model	ALL	TBD		V	
CDM	I-test	±100mA		mA	
Latch-up	Power	Vdd max x 1.5		V	

REGISTER DESCRIPTION

Address	Default	Bits	Register name	Descriptions
00h	78h	[7:0]	chip_id	16-bit sensor model number (read-only), 0x7440
01h	00h	[7:0]		
02h	04h	[7]	pwr_save	Dynamic power save during VBLANK time
		[6]	mech_mod	Single frame capture integration mode with mechanical shutter
		[5]	htest_mod	Horizontal test mode 0b: disabled (default, pixel data displayed) 1b: enabled (black to white data displayed)
		[4]	shut_ctrl	Electronic shutter mode control 0b: shutter disabled, 1b: shutter enabled
		[3:2]	adc_res	ADC resolution selection 00b: 8-bit, 01b: 10-bit, 10b: 12-bit
		[1]	v_flip	Vertical flip control 0b: normal, 1b: vertical flip
		[0]	h_mirr	Horizontal mirror control 0b: normal, 1b: horizontal mirror
03h	00h	[4]	streaming	Active operation mode control 0b: stand-by, 1b: active operation mode
		[2]	pck_inv	PCK polarity inversion 0b: no inversion(default), 1b: inversion
		[1]	row_id_inv	(Reserved)
		[0]	sck_id_inv	(Reserved)
04h	00h	[4]	eds_test_mode	(Factory use only) Pixel accessibility control 0b: default access, 1b: extended access
		[3]	vs_inv	VSYNC polarity inversion 0b: active high, 1b: active low
		[2]	vs_disp	VSYNC display mode 0b: sync mode(default), 1b: data valid mode
		[1]	hs_inv	HSYNC polarity inversion 0b: active high, 1b: active low
		[0]	hs_disp	HSYNC display mode 0b: sync mode(default), 1b: data valid mode
06h	00h	[7:0]	vs_start	VSYNC start position
07h	00h	[7:0]		
08h	00h	[7:0]	vs_width	VSYNC width
09h	01h	[7:0]		
0Ah	00h	[7:0]	hs_start	HSYNC start position
0Bh	00h	[7:0]		
0Ch	00h	[7:0]	hs_width	HSYNC width
0Dh	20h	[7:0]		
0Eh	00h	[7]	psrr_reg_sel	(factory use only)
	04h	[6:4]	psrr_reg_ctrl	(factory use only)
	00h	[2]	srx_en	(factory use only)
	00h	[1]	raw_10_mode	(Reserved)

Address	Default	Bits	Register name	Descriptions
	00h	[0]	avg_sub_smp_en	Average sub_sample en, (s1r_end & s3_end valued need to be controlled) 0b: off , 1b: on
0Fh	29h	[5:4]	max_data_clip_sel	Line ADLC threshold selection
		[3:2]	gain_a	(Reserved)
		[1:0]	gain_b	(Reserved)
10h	00h	[1]	gain_mode	Analog gain mode control 0b: global analog gain, 1b: per channel analog gain
		[0]	glb_gain_mode	Global gain mode control 0b : global sectional gain, 1b: per section gain
11h	00h	[7:0]	analogue_gain_code_global	Global analog gain control when gain_mode=0b
12h	00h	[7:0]	analogue_gain_code_greenR	Analog gain control for Gr
13h	00h	[7:0]	analogue_gain_code_red	Analog gain control for R
14h	00h	[7:0]	analogue_gain_code_blue	Analog gain control for B
15h	00h	[7:0]	analogue_gain_code_greenB	Analog gain control for Gb
16h	0Fh	[4:0]	global_gain_global	(Reserved)
17h	0Fh	[4:0]	global_gain_sec1	Global gain control for section 1
18h	0Fh	[4:0]	global_gain_sec2	Global gain control for section 2
19h	0Fh	[4:0]	global_gain_sec3	Global gain control for sectioin 3
1Ah	0Fh	[4:0]	global_gain_sec4	Global gain control for section 4
1Ch	09h	[7:0]	fine_integration_time[15:0]	Pixel integration time contorl in unit of pixel clock
1Dh	B8h	[7:0]		
1Eh	03h	[7:0]	coarse_integration_time[15:0]	Pixel integration time contorl in unit of line length
1Fh	67h	[7:0]		
20h	07h	[7:0]	frame_length_line[15:0]	Length of frame in unit of line length
21h	D8h	[7:0]		
22h	0Ch	[7:0]	line_length_pck[15:0]	Length of line in unit of data clock
23h	68h	[7:0]		
24h	00h	[7:0]	x_addr_start[11:0]	X-address of the top left corner of the visible pixel data
25h	02h	[7:0]		
26h	00h	[7:0]	y_addr_start[11:0]	Y-address of the top left corner of the visible pixel data
27h	04h	[7:0]		
28h	0Ah	[7:0]	x_addr_end[11:0]	X-address of the bottom right corner of the visible pixel data
29h	39h	[7:0]		
2Ah	07h	[7:0]	y_addr_end[11:0]	Y-address of the bottom right corner of the visible pixel data
2Bh	ABh	[7:0]		
2Ch	0Ah	[7:0]	x_output_size[11:0]	Width of image data output from the sensor
2Dh	30h	[7:0]		
2Eh	07h	[7:0]	y_output_size[11:0]	Height of image data output from the sensor
2Fh	A0h	[7:0]		
30h	01h	[7:0]	x_even_inc[3:0]	Increment in x direction for even pixels - 0, 2, 4, etc.
31h	01h	[7:0]	x_odd_inc[3:0]	Increment in x direction for odd pixels - 1, 3, 5, etc.
32h	01h	[7:0]	y_even_inc[3:0]	Increment in y direction for even pixels - 0, 2, 4, etc.

Address	Default	Bits	Register name	Descriptions
33h	01h	[7:0]	y_odd_inc[3:0]	Increment in y direction for odd pixels - 1, 3, 5, etc.
40h	00h	[0]	offset_mode	(factory use only) Analog offset mode control 0b: global analog offset, 1b: per channel analog offset
41h	80h	[7:0]	offset_global	(factory use only) Global ananlog offset control when offset_mode=0b
42h	80h	[7:0]	offset_gr	(factory use only) Analog offset control for Gr
43h	80h	[7:0]	offset_r	(factory use only) Analog offset control for R
44h	80h	[7:0]	offset_b	(factory use only) Analog offset control for B
45h	80h	[7:0]	offset_gb	(factory use only) Analog offset control for Gb
46h	80h	[7:0]	offset_ref	(factory use only) Analog offset reference control
47h	88h	[7:0]	dvs	(factory use only)
48h	01h	[3]	h_adlc_en	Line-ADLC mode control
		[2]	h_adlc_defect_en	Defect control for above threshold voltage 0b: off, 1b:on
		[1]	h_adlc_ch_sel	channel_h_adld enable 0b: total(default), 1b: channel
		[0]	ob_sel	(Reserved)
49h	00h	[7:0]	even_cnt_del	(Reserved)
4Ah	00h	[7:0]	odd_cnt_del	(Reserved)
4Bh	00h	[7:0]	h_adlc_bpr_thresh	Line ADLC threshold voltage control 00b: 0v (default)
4Ch	77h	[6:4]	read_tx_width_sel	(Reserved)
		[2:0]	shut_tx_width_sel	(Reserved)
4Dh	FFh	[7:4]	s1r_end_val	(Reserved) 0h for avg_sub_sample
		[3:0]	s1s_end_val	(Reserved)
4Eh	F0h	[7:4]	s2_end_val	(Reserved)
		[3:0]	s3_end_val	(Reserved) Fh for avg_sub_sample
4Fh	F7h	[7:4]	s4_end_val	(Reserved)
		[2:0]	savg_end_val	(Reserved)
50h	05h	[7]	pll_op_sel	(Reserved)
		[5:4]	pll_s	(Reserved)
		[3:0]	pll_i	(Reserved)
51h	88h	[7:0]	pll_lpf	(Reserved)
52h	05h	[6]	pll_flten	(Reserved)
		[5]	pll_cppd	(Reserved)
		[4]	auto_tune	(Reserved)
		[3:0]	ivic_tune	(Reserved)
53h	00h	[4]	pll_locked	(Reserved)
		[0]	reserved	(Reserved)
54h	04h	[4:0]	pll_p	Pre PLL clock divider control (can't be read)

Address	Default	Bits	Register name	Descriptions
56h	00h	[9:8]	pll_m	PLL multiplier control (can't be read)
57h	C8h	[7:0]		
58h	02h	[7:4]	vt_sys_div[3:0]	Data clock divider 1 control
	0Ah	[3:0]	vt_pix_div[3:0]	Data clock divider 2 control
59h	02h	[7:4]	op_sys_div[3:0]	Pixel clock divider 1 control
	0Ah	[3:0]	op_pix_div[3:0]	Pixel clock divider 2 control
60h	00h	[1:0]	Scaling mode	0 – No scaling 1 – Horizontal Scaling 2 – Full Scaling (both horizontal and vertical)
61h	10h	[7:0]	scale factor	Down scale factor: M component Range: 16 to upwards , Max : 0xA4
64h	0Ah	[11:8]	fifo_threshold	Threshold level that scaler start to transmit the scaled image when scaling is used. Units : pixels
65h	40h	[7:0]		
70h	33h	[7:4]	i_rmp1	(Reserved)
		[3:0]	i_rmp2	(Reserved)
71h	08h	[6]	crc_output_rev	(Reserved)
		[5]	ramp_sel	(Reserved) ramp type selection 0b=rc ramp(GG:0Fh), 1b=sc ramp(GG:18h)
		[4]	dac_rstr_sel	(Reserved)
		[3:0]	r_ramp	(Reserved)
72h	05h	[4:0]	i_aps	(Reserved)
73h	02h	[2:1]	clp_ctrl	(Reserved)
		[0]	clp_en_ctrl	Analog clamp control 0b: disabled, 1b: enabled
74h	00h	[3:2]	shbn_off	(Reserved)
		[1:0]	pwrdn	(Reserved)
75h	01h	[7:0]	monit	(Reserved)
76h	04h	[7:0]	dblr_tune	Doubler output voltage control 3.0v(default)
77h	C0h	[7]	ld_enable	(Reserved) LD signal enable, 1b(default) = ON
		[6]	bias_sel	(Reserved)
		[5:0]	reserved	(Reserved)
78h	00h	[3]	sda_en	(Reserved)
		[2]	sc1	(Reserved)
		[1]	sc0	(Reserved)
79h	01h	[7]	sync_mode	(Reserved) TG output sync mode
		[6]	bpr_bit_sel	(Reserved)
		[5]	pll_op_lpf	(Reserved)
		[4]	out_hi_z	(Reserved) Output pad to High-Z
		[3]	double_shut	(Reserved)
		[2]	pn9_shift_1bit	(Reserved)
		[1]	loop_back_en	(Reserved)
		[0]	dcen	(Reserved)
7Ah	A5h	[7:6]	YC_SC	(Reserved) IO Driving Strength control

Address	Default	Bits	Register name	Descriptions
		[5:4]	DCLK_SC	(Reserved)
		[3:2]	SCL_SC	(Reserved)
		[1:0]	SDA_SC	(Reserved)
7Bh	00h	[7:5]	ec_comp	(Reserved)
		[4]	func0_sel	(Reserved) TG data output mode
		[3]	avg_vaddr_sel	(Reserved)
		[2]	pn9_shift_1bit	(Reserved)
		[1]	clk_div_sel	(Reserved)
		[0]	test_cursor	(Reserved)
7Ch	0h	[0]	Case shutter	high illumination(cintr 0,1,2) shutter mode 1'b for case shutter ON
7Dh	0x00	[7:0]	sec_offset	(Reserved)
80h	10h	[7]	rvar_efuse_cut_on_even	(Reserved)
		[6]	rvar_ctrl_sel_even	(Reserved)
		[5]	rvar_ramp_sel_even	(factory use only)
		[4:0]	rvar_ctrl_even	(factory use only)
81h	10h	[7]	rvar_efuse_cut_on_odd	(Reserved)
		[6]	rvar_ctrl_sel_odd	(Reserved)
		[5]	rvar_ramp_sel_odd	(factory use only)
		[4:0]	rvar_ctrl_odd	(factory use only)
82h	00h	[7:4]	efuse_cut_time_sel	(Reserved)
		[1]	bpr_efuse_cut_on	(Reserved)
		[0]	bpr_efuse_on	(Reserved)
83h	00h	[4:0]	efuse_x_addr	(Reserved)
84h	00h	[3:0]	efuse_y_addr	(Reserved)
90h	00h	[7:0]	h_addr_reg0	(Reserved)
91h	00h	[7:0]		(Reserved)
92h	00h	[7:0]	v_addr_reg0	(Reserved)
93h	00h	[7:0]		(Reserved)
94h	00h	[7:0]	h_addr_reg1	(Reserved)
95h	00h	[7:0]		(Reserved)
96h	00h	[7:0]	v_addr_reg1	(Reserved)
97h	00h	[7:0]		(Reserved)
98h	00h	[7:0]	h_addr_reg2	(Reserved)
99h	00h	[7:0]		(Reserved)
9Ah	00h	[7:0]	v_addr_reg2	(Reserved)
9Bh	00h	[7:0]		(Reserved)
9Ch	00h	[7:0]	h_addr_reg3	(Reserved)
9Dh	00h	[7:0]		(Reserved)
9Eh	00h	[7:0]	v_addr_reg3	(Reserved)
9Fh	00h	[7:0]		(Reserved)
A0h	00h	[7:0]	h_addr_reg4	(Reserved)
A1h	00h	[7:0]		(Reserved)
A2h	00h	[7:0]	v_addr_reg4	(Reserved)

Address	Default	Bits	Register name	Descriptions
A3h	00h	[7:0]		(Reserved)
A4h	00h	[7:0]	h_addr_reg5	(Reserved)
A5h	00h	[7:0]		(Reserved)
A6h	00h	[7:0]	v_addr_reg5	(Reserved)
A7h	00h	[7:0]		(Reserved)
A8h	00h	[7:0]	h_addr_reg6	(Reserved)
A9h	00h	[7:0]		(Reserved)
AAh	00h	[7:0]	v_addr_reg6	(Reserved)
ABh	00h	[7:0]		(Reserved)
ACh	00h	[7:0]	h_addr_reg7	(Reserved)
ADh	00h	[7:0]		(Reserved)
AEh	00h	[7:0]	v_addr_reg7	(Reserved)
AFh	00h	[7:0]		(Reserved)
B0h	00h	[7:0]	h_addr_reg8	(Reserved)
B1h	00h	[7:0]		(Reserved)
B2h	00h	[7:0]	v_addr_reg8	(Reserved)
B3h	00h	[7:0]		(Reserved)
B4h	00h	[7:0]	h_addr_reg9	(Reserved)
B5h	00h	[7:0]		(Reserved)
B6h	00h	[7:0]	v_addr_reg9	(Reserved)
B7h	00h	[7:0]		(Reserved)
B8h	00h	[7:0]	h_addr_reg10	(Reserved)
B9h	00h	[7:0]		(Reserved)
BAh	00h	[7:0]	v_addr_reg10	(Reserved)
BBh	00h	[7:0]		(Reserved)
BCh	00h	[7:0]	h_addr_reg11	(Reserved)
BDh	00h	[7:0]		(Reserved)
BEh	00h	[7:0]	v_addr_reg11	(Reserved)
BFh	00h	[7:0]		(Reserved)
C0h	00h	[7:0]	h_addr_reg12	(Reserved)
C1h	00h	[7:0]		(Reserved)
C2h	00h	[7:0]	v_addr_reg12	(Reserved)
C3h	00h	[7:0]		(Reserved)
C4h	00h	[7:0]	h_addr_reg13	(Reserved)
C5h	00h	[7:0]		(Reserved)
C6h	00h	[7:0]	v_addr_reg13	(Reserved)
C7h	00h	[7:0]		(Reserved)
C8h	00h	[7:0]	h_addr_reg14	(Reserved)
C9h	00h	[7:0]		(Reserved)
CAh	00h	[7:0]	v_addr_reg14	(Reserved)
CBh	00h	[7:0]		(Reserved)
CCh	00h	[7:0]	h_addr_reg15	(Reserved)
CDh	00h	[7:0]		(Reserved)
CEh	00h	[7:0]	v_addr_reg15	(Reserved)

Address	Default	Bits	Register name	Descriptions
CFh	00h	[7:0]		(Reserved)

IMPORTANT NOTICE

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