DEVICE
PERFORMANCE
SPECIFICATION

KODAK KAF-10010CE Image Sensor

3876 (H) x 2584 (V)
Full-Frame CCD Color Image Sensor
With Square Pixels for Color Cameras

PRELIMINARY

March 24, 2004
Revision F

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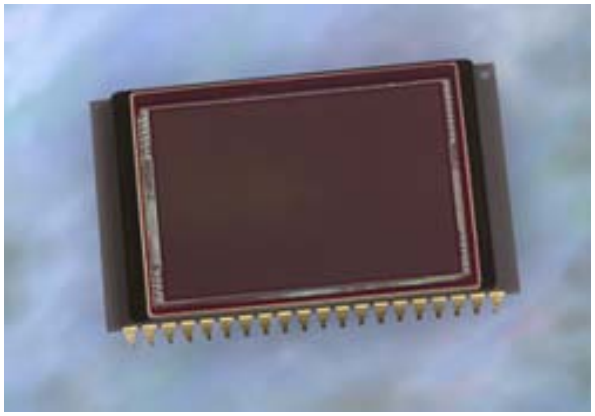
SUMMARY SPECIFICATION

KODAK KAF-10010CE Image Sensor 3876 (H) x 2584 (V) Full-Frame CCD Color Image Sensor



Description

The KAF-10010CE is a 31.7mm diagonal (Type APS+) high performance color full-frame CCD (charge-coupled device) image sensor designed for a wide range of color image sensing applications including digital imaging. Each pixel contains blooming protection by means of a lateral overflow drain thereby preventing image corruption during high light level conditions. Each of the 6.8µm square pixels are patterned with an RGB mosaic color filter with overlying microlenses for improved color response and reproduction. A border of buffer and light-shielded pixels surrounds the photoactive pixels.

Parameter	Typical Value
Architecture	Full Frame CCD; with Square Pixels
Total Number of Pixels	3991 (H) x 2679 (V) = 10.7M
Number of Effective Pixels	3916 (H) x 2624 (V) = 10.3M
Number of Active Pixels	3876 (H) x 2584 (V) = 10.0M
Pixel Size	6.8µm (H) x 6.8µm (V)
Imager Size	31.7mm (diagonal)
Chip Size	29.0mm (H) x 19.1mm (V)
Aspect Ratio	3:2
Saturation Signal	40K e^-
Quantum Efficiency (RGB)	0.34, 0.40, 0.36
Total Sensor Noise	17 e^-
Dark Signal	0.04 mV/s
Dark Current Doubling Temperature	5.8 dC
Linear Dynamic Range	67 dB
Charge Transfer Efficiency	0.999995
Blooming Protection @4ms integration time	1000x saturation exposure
Maximum Data Rate	28 MHz

All parameters above are specified at T =20*C

REVISION NO.: F
EFFECTIVE DATE: March 24, 2004

DEVICE DESCRIPTION

Architecture

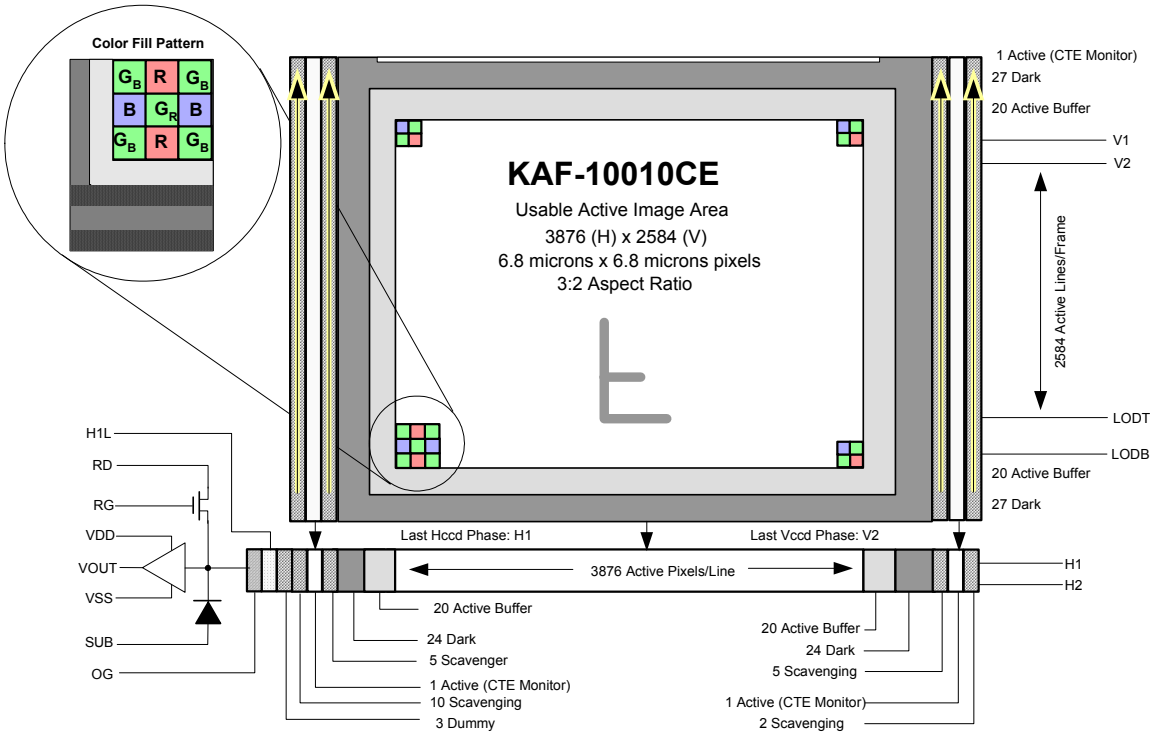


Figure 1 - Sensor Architecture

Dark Reference Pixels

Surrounding the periphery of the device is a border of light shielded pixels creating a dark region. Within this dark region, exist light shielded pixels that include 24 leading and trailing dark pixels on every line. There are also 27 full dark lines at the start and end of every frame. Under normal circumstances, these pixels do not respond to light and may be used as a *dark reference*.

Scavenging Pixels

Within the dark region some pixels are in close proximity to an active pixel, or the light sensitive regions that have been added for manufacturing test purposes, (*CTE Monitor*). In both cases, these pixels can scavenge signal depending on light intensity and wavelength. These pixels should not be used as a dark reference and are called *scavenging pixels*.

Dummy Pixels

Within the horizontal shift register there are 3 leading additional shift phases that are not electrically associated with any columns of pixels within the vertical register. These pixels contain only horizontal shift register dark current signal and do not respond to light and therefore, have been designated as *dummy pixels*. For this reason, they should not be used to determine a dark reference level.

Active Buffer Pixels

Twenty unshielded pixels adjacent to any leading or trailing dark reference regions are classified as active buffer pixels. These pixels are light sensitive but they are not tested for defects and non-uniformities.

CTE Monitor Pixels

Within the horizontal dummy pixel region two light sensitive test pixels (one each on the leading and trailing ends) are added and within the vertical dummy pixel region one light sensitive test pixel has been added. These *CTE monitor pixels* are used for manufacturing test purposes. In order to facilitate measuring the device CTE, the pixels in the CTE Monitor region are coated with blue pigment.

Image Acquisition

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the device. These photon-induced electrons are collected locally by the formation of potential wells at each photogate or pixel site. The number of electrons collected is linearly dependent on light level and exposure time and non-linearly dependent on wavelength. When the pixel's capacity is reached, excess electrons are discharged into the lateral overflow drain to prevent crosstalk or 'blooming'. During the integration period, the V1 and V2 register clocks are held at a constant (low) level.

Charge Transport

The integrated charge from each photogate is transported to the output using a two-step process. Each line (row) of charge is first transported from the vertical CCD's to a horizontal CCD register using the V1 and V2 register clocks. The horizontal CCD is presented a new line on the falling edge of V2 while H1 is held high. The horizontal CCD's then transport each line, pixel by pixel, to the output structure by alternately clocking the H1 and H2 pins in a complementary fashion. A separate connection to the last H1 phase (H1L) is provided to improve the transfer speed of charge to the floating diffusion. On each falling edge of H1 a new charge packet is dumped onto a floating diffusion and sensed by the output amplifier.

Horizontal Register

Output Structure

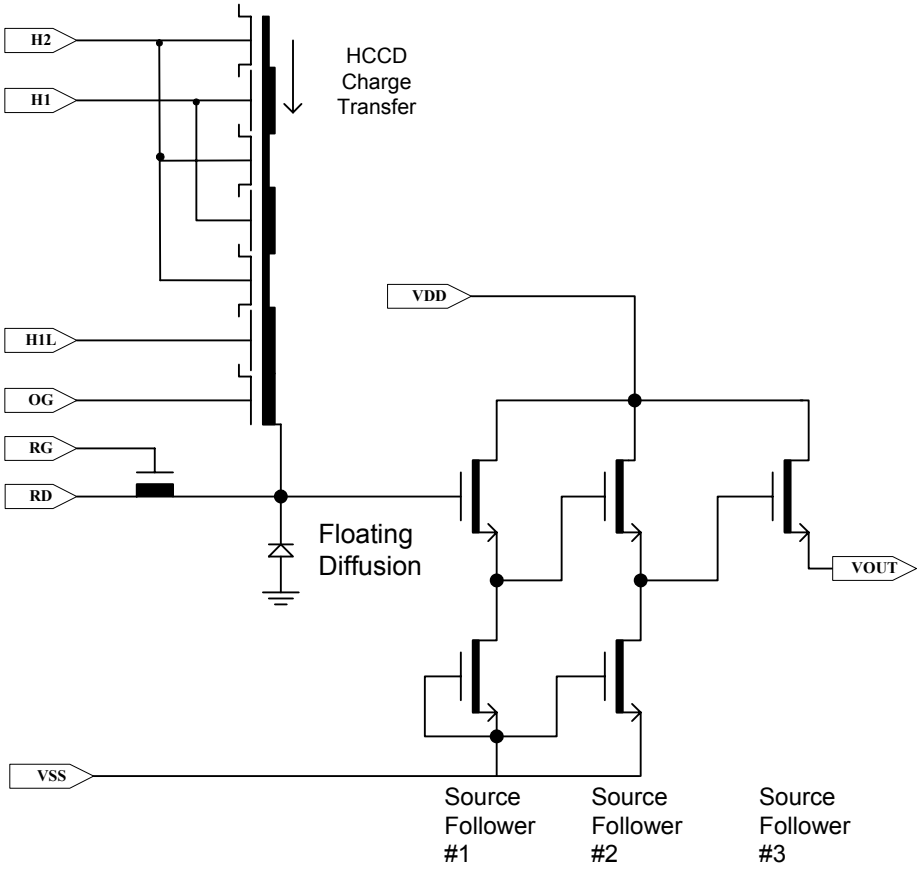


Figure 2 - Output Architecture

Charge presented to the floating diffusion (FD) is converted into a voltage and is current amplified in order to drive off-chip loads. The resulting voltage change seen at the output is linearly related to the amount of charge placed on the FD. Once the signal has been sampled by the system electronics, the reset gate (RG) is clocked to remove the signal and FD is reset to the potential applied by reset drain (RD). Increased signal at the floating diffusion reduces the voltage seen at the output pin. To activate the output structure, an off-chip load must be added to the VOUT pin of the device. See Figure 3.

Output Load

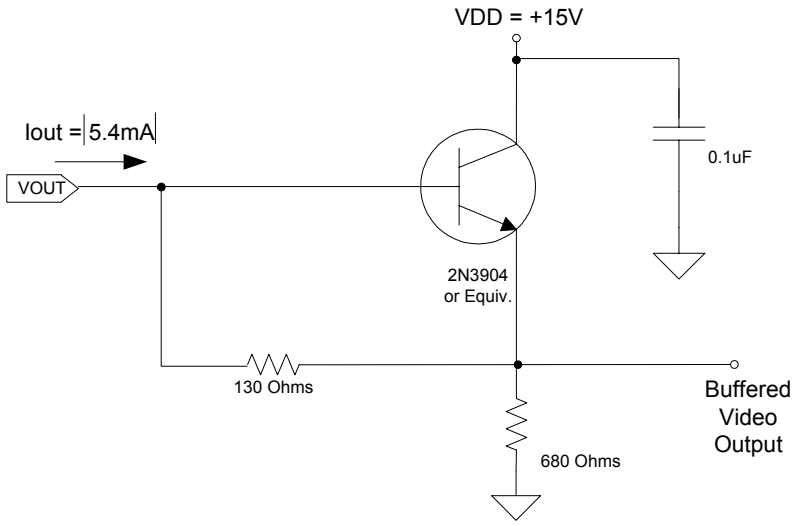


Figure 3 – Recommended Output Structure Load Diagram

Component values may be revised based on operating conditions and other design considerations.

Physical Description

Pin Description and Device Orientation

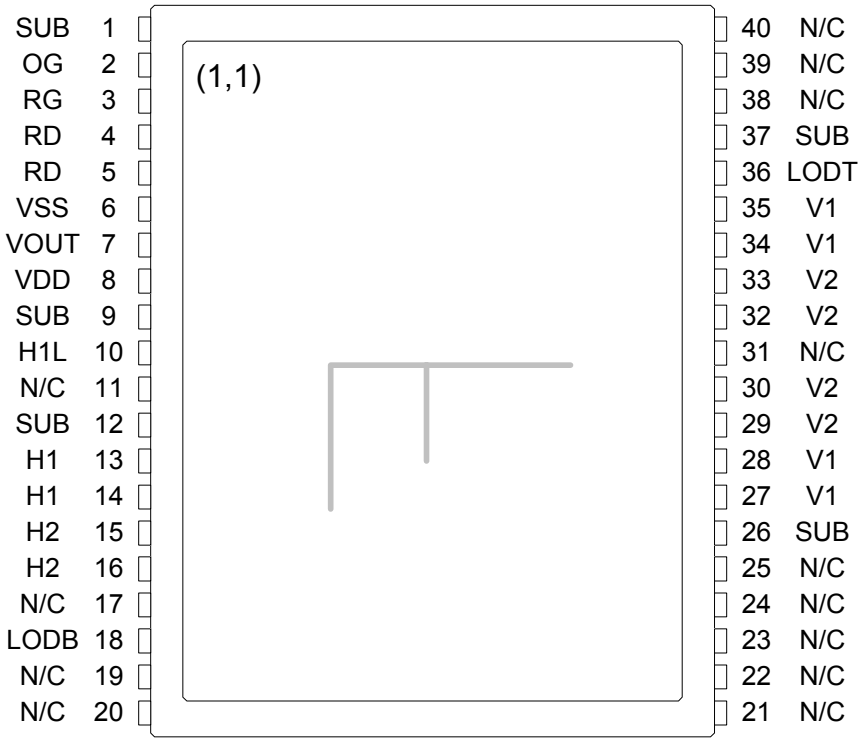


Figure 4 – Package Pin Description

Pin	Name	Description	Pin	Name	Description
1	SUB	Substrate	40	N/C	No Connection
2	OG	Output Gate	39	N/C	No Connection
3	RG	Reset Gate	38	N/C	No Connection
4	RD	Reset Drain	37	SUB	Substrate
5	RD	Reset Drain	36	LODT	Lateral Overflow Drain Top
6	VSS	Output Amplifier Return	35	V1	Vertical Phase 1
7	VOUT	Video Output	34	V1	Vertical Phase 1
8	VDD	Output Amplifier Supply	33	V2	Vertical Phase 2
9	SUB	Substrate	32	V2	Vertical Phase 2
10	H1L	Horizontal Phase 1, Last Gate	31	N/C	No Connection
11	N/C	No Connection	30	V2	Vertical Phase 2
12	SUB	Substrate	29	V2	Vertical Phase 2
13	H1	Horizontal Phase 1	28	V1	Vertical Phase 1
14	H1	Horizontal Phase 1	27	V1	Vertical Phase 1
15	H2	Horizontal Phase 2	26	SUB	Substrate
16	H2	Horizontal Phase 2	25	N/C	No Connection
17	N/C	No Connection	24	N/C	No Connection
18	LODB	Lateral Overflow Drain Bottom	23	N/C	No Connection
19	N/C	No Connection	22	N/C	No Connection
20	N/C	No Connection	21	N/C	No Connection

The pins are on a 0.070” spacing

PERFORMANCE

Image Performance Operational Conditions

Description	Condition - Unless otherwise noted	Notes
Frame time ($t_{readout}$)	1247 msec	Includes overclock pixels
Integration time (t_{int})	250 msec	
Horizontal clock frequency	10 MHz	
Temperature	20°C	
Light source (LED)	Refer to KAF-10010CE Test Plan	Section 2.4
Mode	integrate – readout cycle	

Imaging Performance Specifications

Description	Symbol	Min.	Typ.	Max.	Units	Notes	Sample Plan[16]
Saturation Signal	Vsat	650	700		mV	1	die
Linear Saturation Signal	Ne^-_{sat}	37 K	40K		e^-	1	design
Quantum Effeciency red, green, blue	QE r QE g QE b		34 40 36		%	3	die die die
Photo Response Non-Linearity	PRNL	-10		10	%p-p	2	die
Photo Response Non-Uniformity	PRNU_R PRNU_B/G		12 10	18 15	%p-p	3	die
Dark Signal	DarkSig		0.3	1.5	mV/s	4	die
Dark Signal Non-Uniformity	DSNU		1	3	mV p-p	5	die
Dark Signal Doubling Temperature	ΔT		5.8		°C		design
Total Noise	Dfld_noi		23 0.40	46 0.8	e^- rms mV	6	die
Total Sensor Noise	N		17		e^- rms	15	design
Linear Dynamic Range	DR		67		dB	7	design
Hue Shift	HueUnif		4	10	%	8	die
Horizontal Charge Transfer Efficiency	HCTE	0.99999	0.999995			9	die
Vertical Charge Transfer Efficiency	VCTE	0.99995	0.999999			9	die

Description	Symbol	Min.	Nom.	Max.	Units	Notes	Sample Plan[16]
Blooming Protection	X_ab	1000			x Esat	10	design
DC Offset, output amplifier	Vodc	7.1	7.6	8.1	V	11	die
Output Amplifier Bandwidth	f_{-3dB}	100	118	145	Mhz	12	die
Output Impedance, Amplifier	R_{OUT}	110	135	160	Ohms		die
Hclk Feedthru	V_{hft}	0	30	80	mV	13	die
Reset Feedthru	V_{rft}	500	810	1000	mV	14	design

Notes:

1. Increasing output load currents to improve bandwidth will decrease these values.
2. Worst case deviation, (from 10mV to Vsat min), relative to a linear fit applied between 0 and 500mV exposure. Specified from 20°C to 40°C.
3. Peak to peak non-uniformity test based on an average of 300 x 300 blocks.
4. T=40°C. Average non-illuminated signal with respect to over clocked horizontal register signal.
5. T=40°C. Absolute difference between the maximum and minimum average signal levels of 300 x 300 blocks within the sensor.
6. Dark rms deviation of a multi-sampled pixel as measured using the KAF-10010CE Evaluation Board.
7. 20log(Vsat/N)
8. Gradual variations in hue (red with respect to green pixels and blue with respect to green pixels) in regions of interest of 300 x 300 blocks.
9. Measured per transfer at 80% of Vsat.
10. Esat equals the exposure required to achieve saturation. X_b represents the number of Esat exposures the sensor can tolerate before failure. Specified at 4 msec.
11. Video level DC offset with respect to ground at clamp position.
12. Last stage only. CLOAD = 10pF. Then f_{-3dB} = (1 / (2π*ROUT*CLOAD)).
13. Amount of artificial signal due to H1 coupling.
14. Amplitude of feedthrough pulse in VOUT due to RG coupling.
15. Calculated value subtracting the noise contribution from the KAF-10010CE Evaluation Board as 15 electrons rms.
16. Sampling plan defined as “die” indicates that every device is verified against the specified performance limits. Sampling plan defined as “design” indicates a sampled test or characterization, at the discretion of Kodak, against the specified performance limits.

Typical Performance Curves

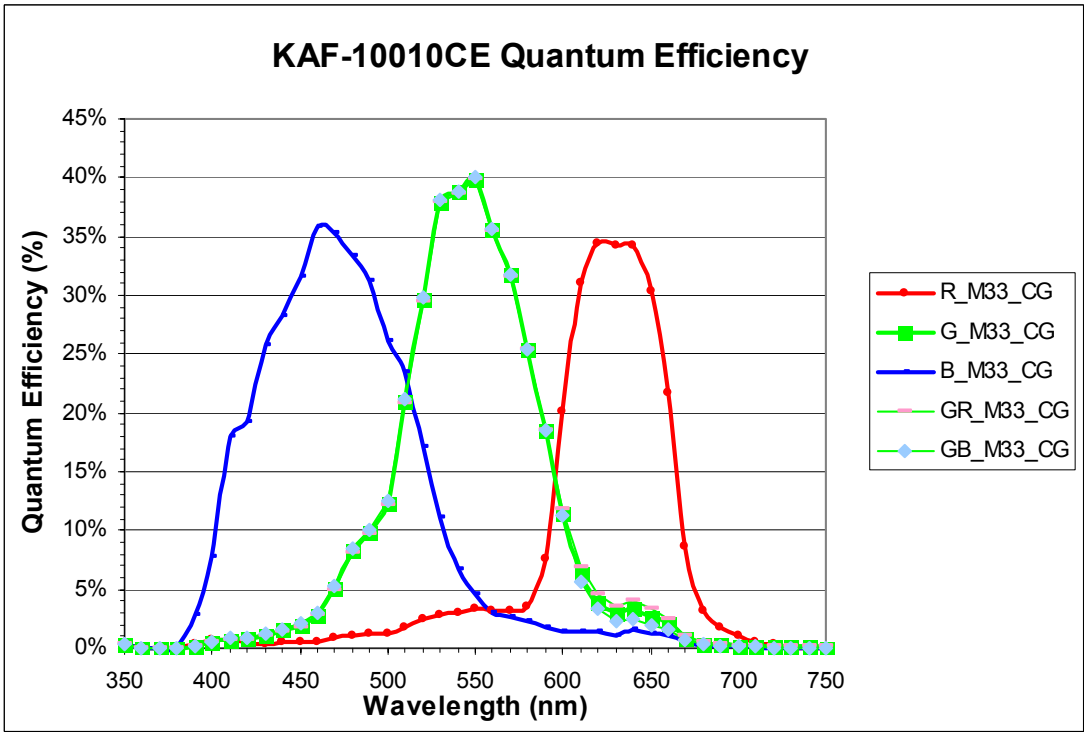


Figure 5 – Estimated Quantum Efficiency

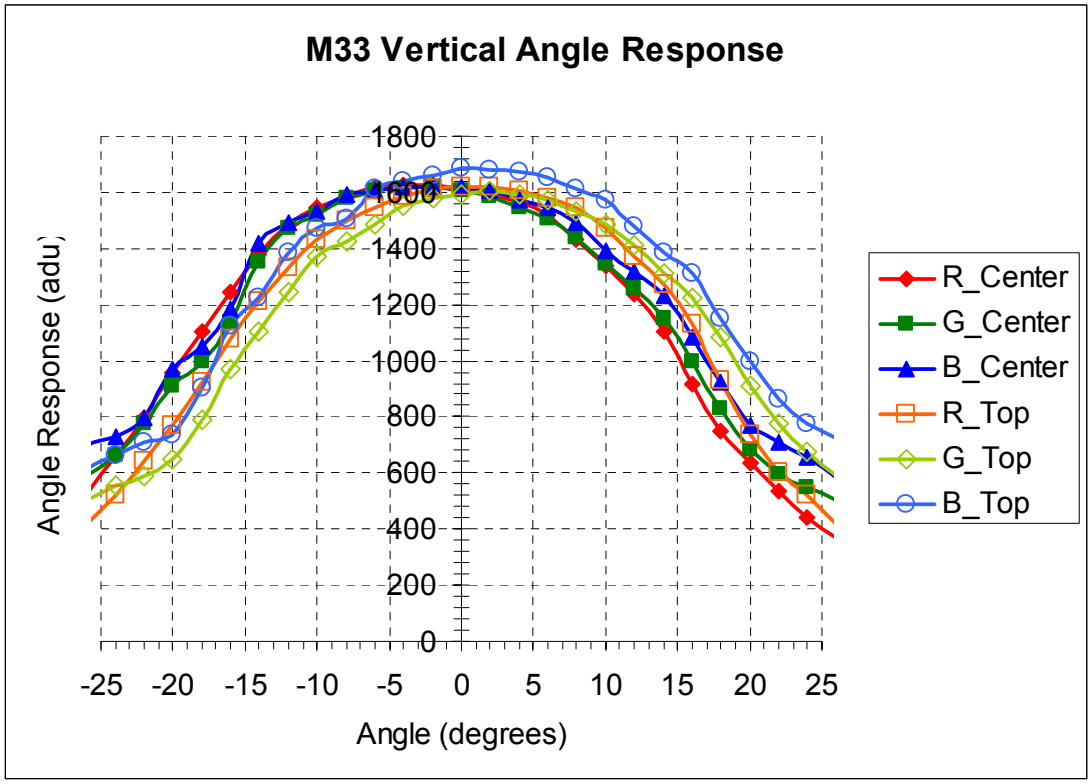


Figure 6 – Typical Vertical Angular Response

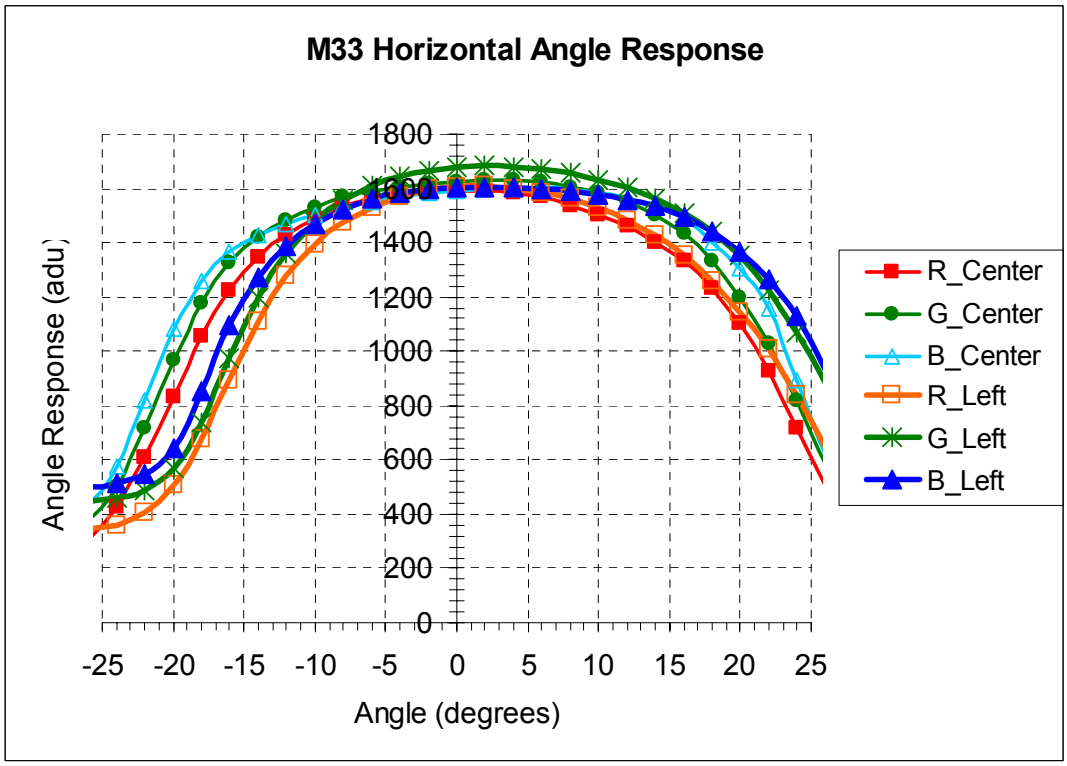


Figure 7 – Typical Horizontal Angular Response

Defect Definitions

Defect Operational Conditions

All defect tests performed at T=20°C, t_{int} = 250 msec and $t_{readout}$ = 1247 msec

Defect Specifications

Classification	Points	Clusters	Columns
Standard Quality (SQ)	≤2500	≤30	≤10

Point Defects

A pixel which deviates by more than 7mV above or below neighboring pixels under non-illuminated conditions

-- OR --

A pixel which deviates by more than 7% above or 11% below neighboring pixels under illuminated conditions

Cluster Defect

A grouping of not more than 10 adjacent point defects

Cluster defects are separated by no less than 4 good pixels in any direction

Column Defect

A grouping of 6 or more point defects along a single column

-- OR --

A column which deviates by more than 0.7mV above or below neighboring columns under non-illuminated conditions

-- OR --

A column which deviates by more than 1.5% above or below neighboring columns under illuminated conditions

Column defects are separated by no less than 4 good columns. No double (or more) column defects will be permitted.

Column and cluster defects are separated by at least 4 good columns in the x direction.

Dead Columns

A column which deviates by more than 50% below neighboring columns under illuminated conditions

Saturated Columns

A column which deviates by more than 100mV above neighboring columns under non-illuminated conditions. No saturated columns are allowed

TEST DEFINITIONS

The test description document is a supplement to this device performance specification. Refer to the latest revision of the KAF-10010CE Test Plan document for test conditions and definitions.

OPERATION

Absolute Maximum Ratings

Description[10]	Symbol	Minimum	Maximum	Units	Notes
Diode Pin Voltages	V_{diode}	-0.3	38	V	1,2
Gate Pin Voltages - Type 1	V_{gate1}	-44	44	V	1,3
Gate Pin Voltages - Type 2	V_{gate2}	-0.3	22	V	1,4
Overlapping Gate Voltages	V_{1-2}		35	V	5
Non-overlapping Gate Voltages	V_{g-g}		45	V	6
V1, V2 – LOD Voltages	V_{V-L}		41	V	7
Output Bias Current	I_{out}		-30	mA	8
LOD Diode Voltage	V_{LOD}	-0.3	55	V	9
ESD Well Voltage	V_{WELL}	----	----	V	11

Notes:
1. Referenced to pin SUB
2. Includes pins: RD, VDD, VSS, VOUT.
3. Includes pins: V1, V2, H1, H1L, H2.
4. Includes pins with ESD protection: RG, OG.
5. Voltage difference between overlapping gates. Includes: V1 to V2; H1, H1L to H2; H1L to OG; V1 to H2.
6. Voltage difference between non-overlapping gates. Includes: V1 to H1, H1L; V2, OG to H2.
7. Voltage difference between V1, V2 gates and LODT, LODB diode.
8. Avoid shorting output pins to ground or any low impedance source during operation. Amplifier bandwidth increases at higher currents and lower load capacitance at the expense of reduced gain (sensitivity). Operation at these values will reduce MTTF.
9. V1, H1, V2, H2, H1L, OG, and RD are tied to 0V.
10. Absolute maximum rating is defined as a level or condition that should not be exceeded at any time per the description. If the level or condition is exceeded, the device will be degraded and may be damaged.
11. Leave this pin not connected (floating).

Power-up Sequence

The sequence chosen to perform an initial power-up is not critical for device reliability. A coordinated sequence may minimize noise and the following sequence is recommended:

1. Connect the ground pins (SUB).
2. Supply the appropriate biases and clocks to the remaining pins.

DC Bias Operating Conditions

Description	Symbol	Minimum	Nominal	Maximum	Units	Maximum DC Current (mA)	Notes
Reset Drain	RD	11.3	11.5	11.7	V	I_{RD} = 0.01	
Output Amplifier Return	VSS	1.05	1.25	1.45	V	I_{SS} = -3.0	
Output Amplifier Supply	VDD	14.5	15.0	15.5	V	I_{OUT} + I_{SS}	
Substrate	SUB		GND		V	-0.01	2
Output Gate	OG	-2.7	-2.5	-2.3	V	0.1	
Lateral Drain	LODT, LODB	9.5	10.0	10.5	V	0.2	2
Video Output Current	I_{OUT}	-3	-5	-8	mA		1
ESD Well Bias	V_{WELL}		----		V		3

Notes:
1. An output load sink must be applied to VOUT to activate output amplifier - see Figure 3.
2. Maximum current expected up to saturation exposure (Esat).
3. Leave this pin not connected (floating).

AC Operating Conditions

Clock Levels

Description	Symbol	Level	Minimum	Nominal	Maximum	Units	Effective Capacitance	Notes
V1 Low Level	V1L	Low	-9.5	-9.0	-8.5	V	200 nF	1
V1 High Level	V1H	High	2.0	2.5	3.0	V		1
V2 Low Level	V2L	Low	-9.5	-9.0	-8.5	V	200 nF	1
V1 High Level	V2H	High	2.0	2.5	3.0	V		1
H1 Low Level	H1L	Low	-4.7	-4.5	-4.3	V	400 pF	1
H1 High Level	H1H	High	1.3	1.5	1.7	V		1
H1L Low Level	$H1L_{low,}$	Low	-6.7	-6.5	-6.3	V	10 pF	1
H1L High Level	$H1L_{high}$	High	1.3	1.5	1.7	V		1
H2 Low Level	H2L	Low	-5.2	-5.0	-4.8	V	300 pF	1
H2 High Level	H2H	High	0.8	1.0	1.2	V		1
RG Low Level	RGL	Low	-0.2	0.0	0.2	V	7 pF	1
RG High Level	RGH	High	5.8	6.0	6.2	V		1

Notes:
1. All pins draw less than 10μA DC current. Capacitance values relative to SUB (substrate).

Timing Requirements

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
H1, H2 Clock Frequency	f_H			28	MHz	1, 2
V1, V2 Clock Frequency	f_V			83.3	kHz	1, 2
Pixel Period (1 Count)	t_e	35.7			ns	2
H1, H2 Setup Time	t_{HS}	1			µs	
H1L – VOUT Delay	t_{HV}		2		ns	
RG - VOUT Delay	t_{RV}		2		ns	
Readout Time	$t_{readout}$	416.8			ms	4, 5
Integration Time	t_{int}					3, 4
Line Time	t_{line}	155.6			µs	4
Flush Time	t_{flush}	32.4			ms	
V1, V2 Clock Pulse Width	t_V	6			µs	2

Notes:

1. 50% duty cycle values.
2. CTE will degrade above the nominal frequency.
3. Integration time is user specified.
4. Longer times will degrade noise performance.
5. $t_{readout} = t_{line} * 2679$ lines.

TIMING DIAGRAMS

Frame Timing

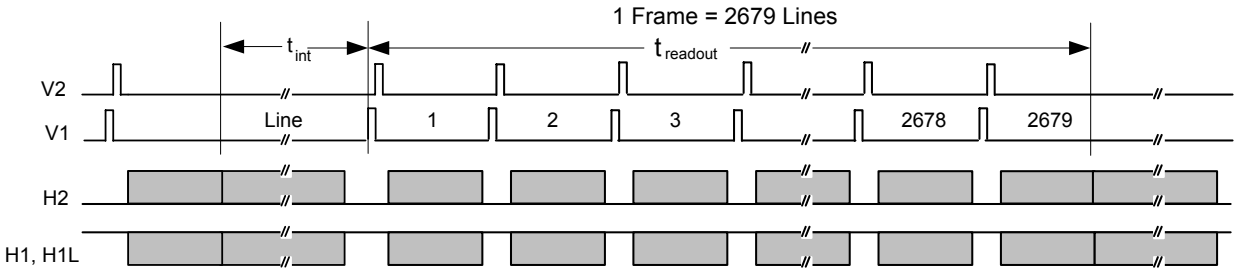


Figure 8 - Frame Timing

Line Timing

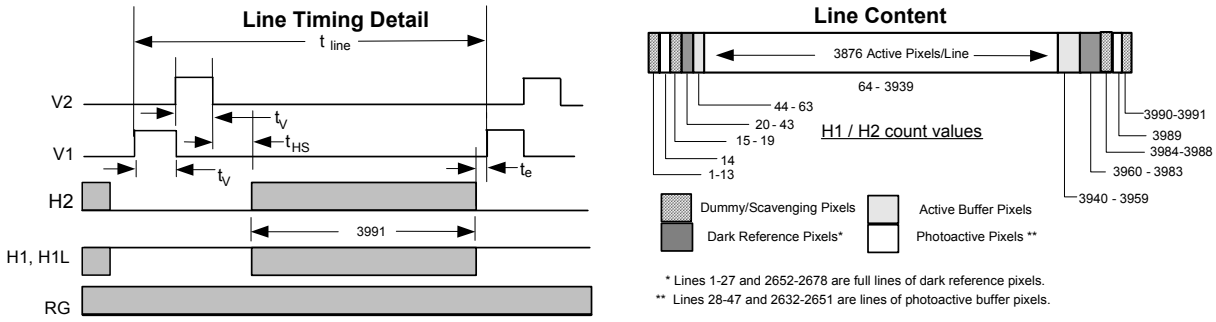


Figure 9 - Line Timing and content

Pixel Timing

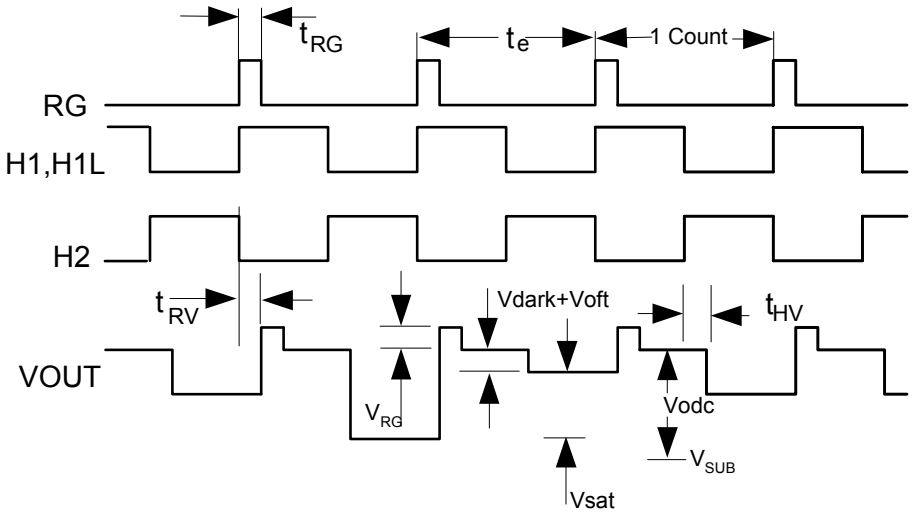


Figure 10 – Pixel Timing

MODE OF OPERATION

Power-up Flush Cycle

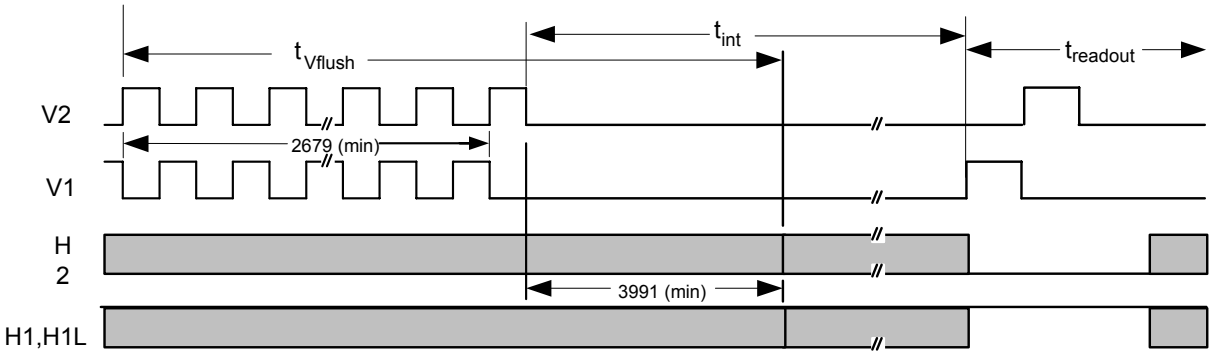


Figure 11 – Power-up Flush Cycle

STORAGE AND HANDLING

Environmental Conditions

Description	Symbol	Minimum	Maximum	Units	Notes
Humidity	RH	5	90	%	1
Storage Temperature	T_{ST}	-20	80	°C	2
Operating Temperature	T_{OP}	-10	70	°C	3
Guaranteed Temperature of Performance	T_{SP}	20	40	°C	4

Notes:
1. T=25°C. Excessive humidity will degrade MTTF.
2. Long-term storage toward the maximum temperature will accelerate color filter degradation.
3. Noise performance will degrade at higher temperatures.
4. See section for Imaging Performance Specifications.

Handling Conditions

ESD

1. This device contains limited protection against Electrostatic Discharge (ESD). CCD image sensors can be damaged by electrostatic discharge. Failure to do so may alter device performance and reliability.
2. Devices should be handled in accordance with strict ESD procedures for class TBD devices.
3. Devices are shipped in static-safe containers and should only be handled at static-safe workstations.
4. See Application Note MTD/PS-0224 for proper handling and grounding procedures. This application note also contains recommendations for workplace modifications for the minimization of electrostatic discharge.
5. Store devices in containers made of electro-conductive materials.

Soldering recommendations

1. The soldering iron tip temperature is to not exceed 370 °C. Failure to do so may alter device performance and reliability.
2. Flow soldering method is not recommended. Solder dipping can cause damage to the glass and harm the imaging capability of the device. Recommended method is by partial heating. Kodak recommends the use of a grounded 30W soldering iron. Heat each pin for less than 2 seconds duration.

3. For circuit board repair, or de-soldering an image sensor, do not use solder suction equipment. In any instance, care should be given to minimize and eliminate electrostatic discharge.

Cover glass care and cleanliness

1. Devices are shipped free of mobile contamination inside the package cavity. Immovable particles and scratches that are within the imager pixel area and the corresponding cover glass region directly above the pixel sites are also not allowed.
2. The cover glass is highly susceptible to particles and other contamination. Perform all assembly operations in a certified clean room of class 1000 or less.
3. Touching the cover glass must be avoided. Improper cleaning of the cover glass may damage these devices. Refer to Application Note MTD/PS-0237 “Cover Glass Cleaning Procedure for Image Sensors”
4. Devices are shipped with the cover glass region covered with a protective tape. The tape should be removed upon usage.

Environmental Exposure

1. Do not expose to strong sun light for long periods of time. The color filters may become discolored. Long time exposures to a static high contrast scene should be avoided. The image sensor may become discolored and localized changes in response may occur from color filter aging.
2. Exposure to temperatures exceeding the absolute maximum levels should be avoided for storage and operation. Color filter performance may be degraded. Failure to do so may alter device performance and reliability.
3. Avoid sudden temperature changes.
4. Exposure to excessive humidity will affect device characteristics and should be avoided. Failure to do so may alter device performance and reliability.
5. Avoid storage of the product in the presence of dust or corrosive agents or gases.
6. Long-term storage should be avoided. Deterioration of lead solderability may occur. It is advised that the solderability of the device leads be re-inspected after an extended period of storage, over one year.

MECHANICAL DRAWINGS

Package

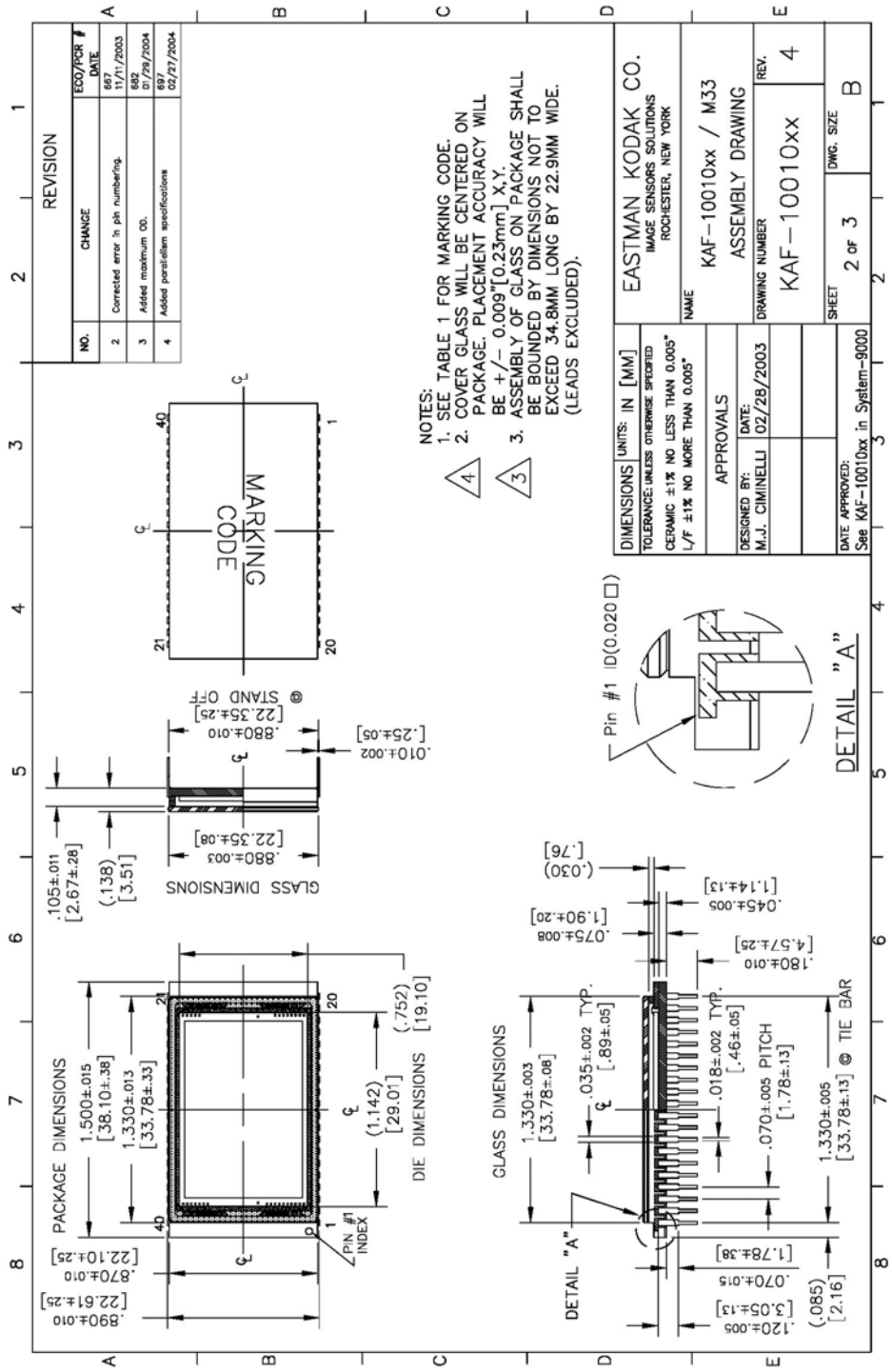


Figure 12 - Package Drawing

Coverglass

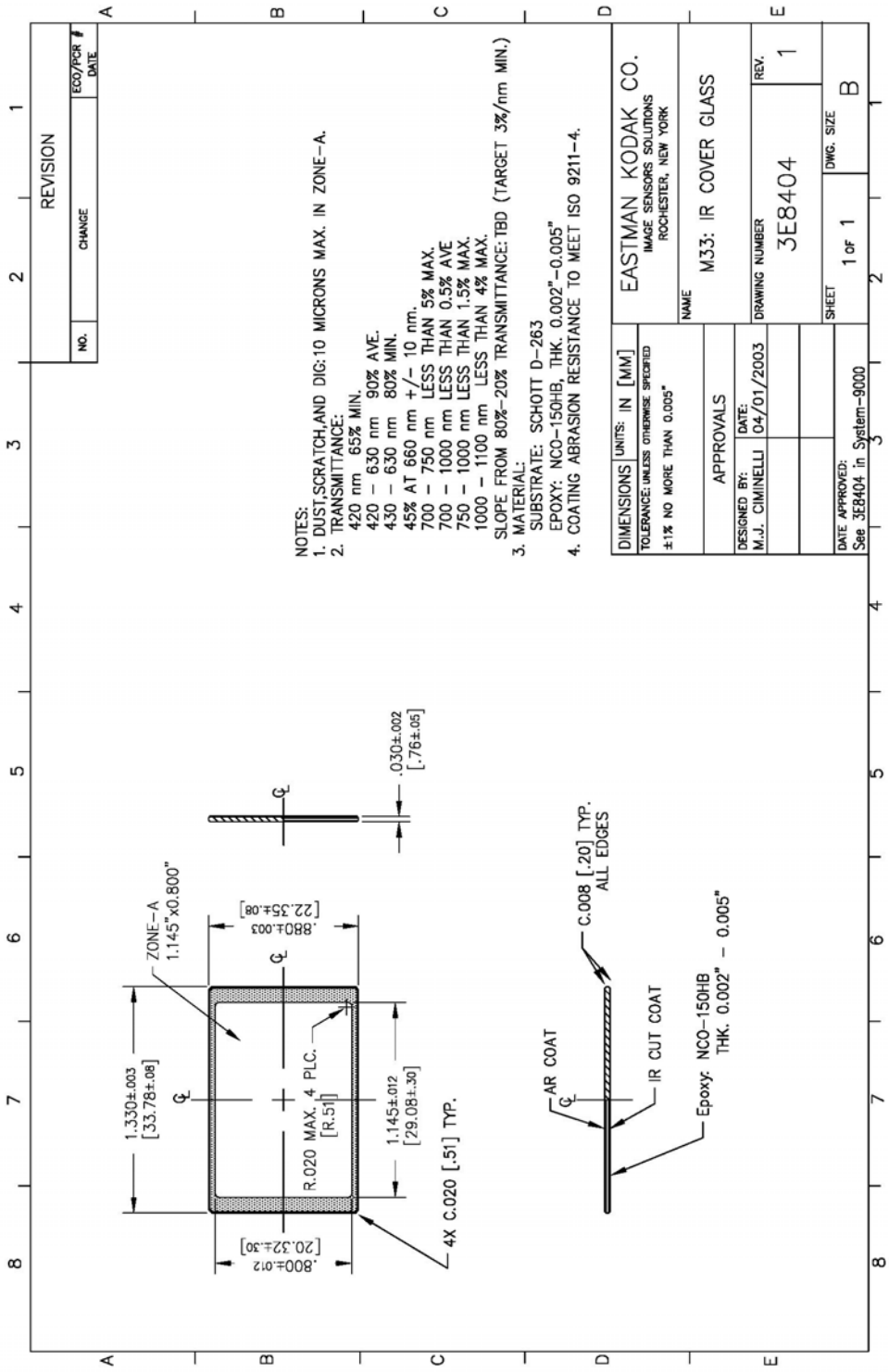


Figure 13 – Cover Glass Drawing

QUALITY ASSURANCE AND RELIABILITY

Quality Strategy: All image sensors will conform to the specifications stated in this document. This will be accomplished through a combination of statistical process control and inspection at key points of the production process. Typical specification limits are not guaranteed but provided as a design target. For further information refer to ISS Application Note MTD/PS-0292, Quality and Reliability.

Replacement: All devices are warranted against failure in accordance with the terms of Terms of Sale. This does not include failure due to mechanical and electrical causes defined as the liability of the customer below.

Liability of the Supplier: A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer.

Liability of the Customer: Damage from mechanical (scratches or breakage), electrostatic discharge (ESD) damage, or other electrical misuse of the device beyond the stated absolute maximum ratings, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.

Reliability: Information concerning the quality assurance and reliability testing procedures and results are available from the Image Sensor Solutions and can be supplied upon request. For further information refer to ISS Application Note MTD/PS-0292, Quality and Reliability.

Test Data Retention: Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.

Mechanical: The device assembly drawing is provided as a reference. The device will conform to the published package tolerances.

ORDERING INFORMATION

Available Part Configurations

Type	Description	Glass Configuration
KAF-10010CE	Color with microlens	IR, sealed

Please contact Image Sensor Solutions for available part numbers.

Address all inquiries and purchase orders to:

Image Sensor Solutions
Eastman Kodak Company
Rochester, New York 14650-2010
Phone: (585) 722-4385
Fax: (585) 477-4947
E-mail: imagers@kodak.com

Kodak reserves the right to change any information contained herein without notice. All information furnished by Kodak is believed to be accurate.

WARNING: LIFE SUPPORT APPLICATIONS POLICY

Kodak image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of the Eastman Kodak Company. Product warranty is limited to replacement of defective components and does not cover injury or property or other consequential damages.

REVISION CHANGES

Revision Number	Description of Changes
A	Preliminary Specification. Initial Release.
B	Changed OG operating condition from 1.25V to –2.0V. Updated QE data and added coverglass drawing. Changed test block size from 147 x 147 pixels to 300 x 300 pixels.
C	Updated parameter table on pg. 3 (chip size, Dark Sig. & DR). Updated pinout and added pixel (1,1) location in Figure 4. Updated imaging performance specification table (QE, PRNL, PRNU, Dfld_noise, Dynamic Range, f_{-3dB}, V_{hft}). Updated QE curve. Removed Typical Blooming Performance chart. Updated the timing requirements table. Updated package and coverglass drawings.
D	Updated released version of package and coverglass drawings. Inserted value for flush time.
E	Updated performance specifications with measured characterization data, Increased QE numbers, modified dark signal doubling temperature to 5.8°C, Modified Vodc limits based on test data, Updated Rout and f_{-3dB} values based on test data. Added new QE figure, Modified OG voltage values in the DC operating conditions table. Increased V clock High values and added clock capacitance values in the AC Operating conditions Clock level table. Increased the HCLK frequency to 28MHz in the Timing requirements table. Also, updated the pixel period, line time and readout time based on this change.
F	Added device photo and updated max data rate on pg.3. Upgated imaging performance specifications on pg10: Added min Vsat/Nsat limit. Added min PRNL limit. Increased PRNU_Red typ. & max limit to 12% & 18% respectively. Reduced max Noise limit to 0.8mV (46e-rms). Added typical HCTE and typ. & min. VCTE. Added Fig. 6 and Fig.7 for vertical and horizontal Angle QE. Updated package drawing based on new assembly drawing.